



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:

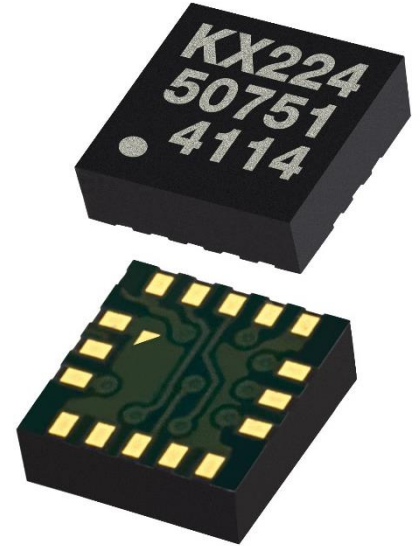
KX224-1053

Rev. 1.0

26-Sep-16

Product Description

The KX224-1053 is a tri-axis ±8g, ±16g or ±32g silicon micromachined accelerometers with integrated 2048 byte buffer, orientation, tap/double tap, activity detecting, and Free fall algorithms. The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning, and intelligent user-programmable application algorithms. The accelerometer is delivered in a 3 x 3 x 0.9 mm LGA plastic package operating from a 1.71V – 3.6V DC supply. Voltage regulators are used to maintain constant internal operating voltages over the range of input supply voltages. This results in stable operating characteristics over the range of input supply voltages. I²C or SPI digital protocol is used to communicate with the chip to configure and check for updates to the orientation, Directional Tap™ detection, Free fall detection and activity monitoring algorithms.



Features

- 3 x 3 x 0.9 mm LGA
- User-selectable g Range up to ± 32g
- User-selectable Output Data Rate up to 25600Hz
- User-selectable low power or high resolution mode
- Digital High-Pass Filter Outputs
- Extra large embedded 2048 byte FIFO/FILO buffer
- Low Power Consumption with FlexSet™ Performance Optimization
- Internal voltage regulator
- Enhanced integrated Free fall, Directional Tap/Double-Tap™, and Device-orientation Algorithms
- User-configurable wake-up function
- Digital I²C up to 3.4MHz
- Digital SPI up to 10MHz
- Lead-free Solderability
- Excellent Temperature Performance
- High Shock Survivability
- Factory Programmed Offset and Sensitivity
- Self-test Function


	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

Table of Contents

PRODUCT DESCRIPTION	1
FEATURES	1
TABLE OF CONTENTS	2
FUNCTIONAL DIAGRAM	6
PRODUCT SPECIFICATIONS	7
MECHANICAL	7
ELECTRICAL	8
<i>Start Up Time Profile</i>	9
<i>Current Profile</i>	9
<i>Power-On Procedure</i>	10
ENVIRONMENTAL	11
TERMINOLOGY	12
<i>g</i>	12
<i>Sensitivity</i>	12
<i>Zero-g offset</i>	12
<i>Self-test</i>	12
FUNCTIONALITY	13
<i>Sense element</i>	13
<i>ASIC interface</i>	13
<i>Factory calibration</i>	13
APPLICATION SCHEMATIC AND PIN DESCRIPTION	14
<i>Application Schematic</i>	14
<i>Pin Descriptions</i>	14
PACKAGE DIMENSIONS AND ORIENTATION	15
<i>Dimensions</i>	15
<i>Orientation</i>	16
DIGITAL INTERFACE	18
I ² C SERIAL INTERFACE	18
<i>I²C Operation</i>	19
<i>Writing to accelerometer's 8-bit Register</i>	21
<i>Reading from accelerometer's 8-bit Register</i>	21
<i>Data Transfer Sequences</i>	22
<i>HS-mode</i>	23
<i>I²C Timing Diagram</i>	24
SPI COMMUNICATIONS	25
<i>4-Wire SPI Interface</i>	25
<i>4-Wire SPI Timing Diagram</i>	26
<i>4-Wire Read and Write Registers</i>	27

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

3-Wire SPI Interface..... 28
3-Wire SPI Timing Diagram 29
3-Wire Read and Write Registers 30

EMBEDDED REGISTERS.....31

ACCELEROMETER OUTPUTS..... 32
XHP_L..... 33
XHP_H..... 33
YHP_L..... 33
YHP_H..... 33
ZHP_L..... 34
ZHP_H..... 34
XOUT_L..... 34
XOUT_H..... 34
YOUT_L..... 35
YOUT_H..... 35
ZOUT_L..... 35
ZOUT_H..... 35
COTR..... 36
WHO_AM_I..... 36
TSCP..... 36
TSPP..... 37
INS1..... 37
INS2..... 38
INS3..... 39
STATUS_REG..... 40
INT_REL..... 40
CNTL1..... 40
CNTL2..... 41
CNTL3..... 43
ODCNTL..... 45
INC1..... 46
INC2..... 47
INC3..... 47
INC4..... 48
INC5..... 48
INC6..... 49
TILT_TIMER..... 50
WUFC..... 50
TDTRC..... 50
TDTC..... 51
TTH..... 51
TTL..... 52
FTD..... 52



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

STD 52

TLT..... 53

TWS..... 53

FFTH 54

FFC 54

FFCNTL 54

ATH 55

TILT_ANGLE_LL 55

TILT_ANGLE_HL..... 56

HYST_SET 56

LP_CNTL 56

BUF_CNTL1 57

BUF_CNTL2 58

BUF_STATUS_1 59

BUF_STATUS_2 59

BUF_CLEAR 59

BUF_READ..... 60

SELF_TEST 60

EMBEDDED APPLICATIONS 61

 ORIENTATION DETECTION FEATURE..... 61

Hysteresis..... 61

Device Orientation Angle (aka Tilt Angle)..... 62

Tilt Timer..... 63

 MOTION INTERRUPT FEATURE DESCRIPTION 64

 DIRECTIONAL TAP DETECTION FEATURE DESCRIPTION 66

Performance Index..... 66

Single Tap Detection..... 67

Double Tap Detection 68

 FREE FALL DETECT..... 69

 SAMPLE BUFFER FEATURE DESCRIPTION 71

FIFO Mode 71

Stream Mode..... 71

Trigger Mode 72

FILO Mode 72

Buffer Operation..... 72

REVISION HISTORY 78

NOTICE..... 79


 PRECAUTION ON USING KIONIX PRODUCTS 79

 PRECAUTION FOR MOUNTING / CIRCUIT BOARD DESIGN..... 80

 PRECAUTIONS REGARDING APPLICATION EXAMPLES AND EXTERNAL CIRCUITS 80

 PRECAUTION FOR ELECTROSTATIC 80

 PRECAUTION FOR STORAGE / TRANSPORTATION 80

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

PRECAUTION FOR PRODUCT LABEL 81

PRECAUTION FOR DISPOSITION 81

PRECAUTION FOR FOREIGN EXCHANGE AND FOREIGN TRADE ACT 81

PRECAUTION REGARDING INTELLECTUAL PROPERTY RIGHTS 81

OTHER PRECAUTION..... 81

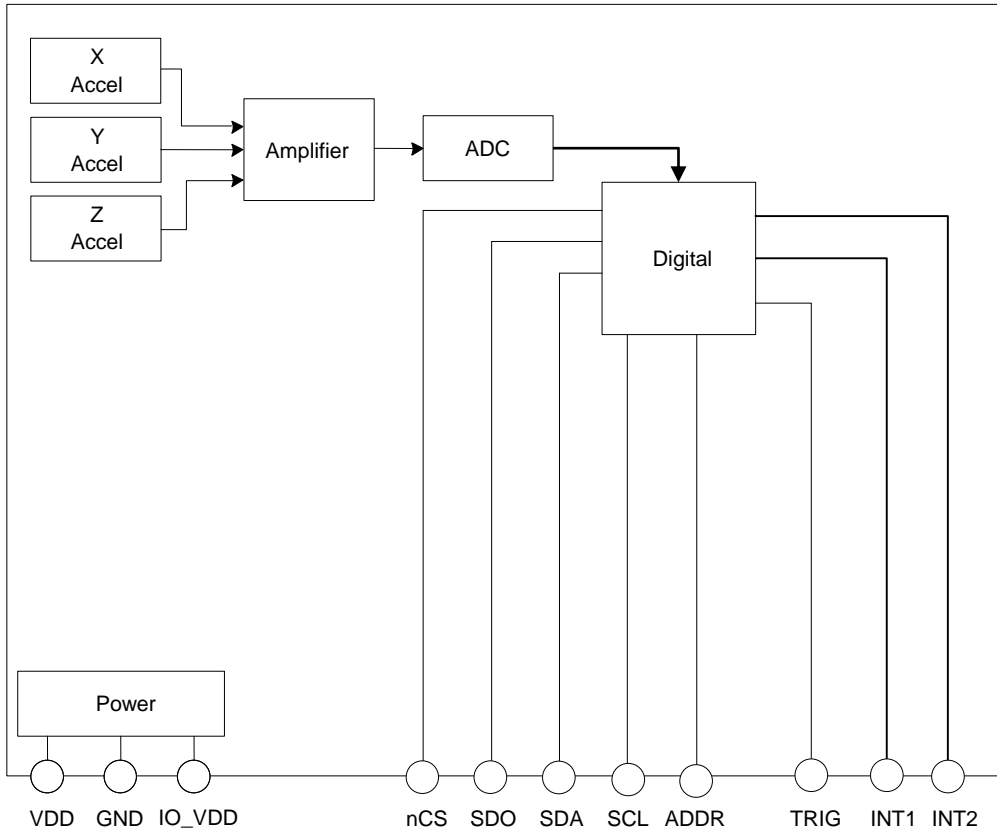
GENERAL PRECAUTION 81




± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

Functional Diagram



	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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Product Specifications

Mechanical


(specifications are for operation at VDD = 2.5V and T = 25°C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		°C	-40	-	85
Zero-g Offset		mg		±75	±175
Zero-g Offset Variation from RT over Temp.		mg/°C		0.5	
Sensitivity ¹	GSEL1=0, GSEL0=0 (±8g)	counts/g	3768	4096	4424
	GSEL1=0, GSEL0=1 (± 16g)		1884	2048	2212
	GSEL1=1, GSEL0=0 (± 32g)		942	1024	1106
Sensitivity (Buffer 8-bit mode) ^{1,2}	GSEL1=0, GSEL0=0 (± 8g)	counts/g	15	16	17
	GSEL1=0, GSEL0=1 (± 16g)		7	8	9
	GSEL1=1, GSEL0=0 (± 32g)		3	4	5
Sensitivity Variation from RT over Temp.		%/°C		0.01	
Positive Self Test Output change on Activation ⁵		g		0.5	
Mechanical Resonance (-3dB) ³		Hz		XY 6000 Z 3600	
Non-Linearity		% of FS		0.6	
Cross Axis Sensitivity		%		2	
Noise (with low-pass filter = ODR/9) ⁴		$\mu\text{g} / \sqrt{\text{Hz}}$		XY 750 Z 1200	

Table 1: Mechanical Specifications

Notes:

1. Resolution and acceleration ranges are user selectable via I²C or SPI.
2. Sensitivity is proportional to BRES in BUF_CNTL2.
3. Resonance as defined by the dampened mechanical sensor.
4. Noise varies with Output Data Rate (ODR) and Current Consumption settings. Please consult [FlexSet™ Performance Optimization Tool](#) for additional details.
5. Requires changing of STPOL bit in INC1 register to 1 prior to performing self-test

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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Electrical

(specifications are for operation at VDD = 2.5V and T = 25°C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Operating	V	1.71	2.5	3.6
I/O Pads Supply Voltage (IO_VDD)		V	1.7		VDD
Current Consumption	High Resolution Mode (RES = 1)	μA		145	
	Low Power Mode ¹ (RES = 0)			10	
	Standby			0.9	
Output Low Voltage (IO_VDD < 2V) ²		V	-	-	0.2 * IO_VDD
Output Low Voltage (IO_VDD ≥ 2V) ²		V	-	-	0.4
Output High Voltage		V	0.8 * IO_VDD	-	-
Input Low Voltage		V	-	-	0.2 * IO_VDD
Input High Voltage		V	0.8 * IO_VDD	-	-
Input Pull-down Current		μA		0	
Start Up Time ³		ms	2.0		1300
Power Up Time ⁴		ms		20	50
I ² C Communication Rate		MHz			3.4
SPI Communication Rate		MHz			10
Output Data Rate (ODR) ⁵		Hz	0.781	50	25600
Bandwidth (-3dB) ⁶	RES = 0	Hz		800	
	RES = 1	Hz		ODR/2	

Table 2: Electrical Specifications

Notes:

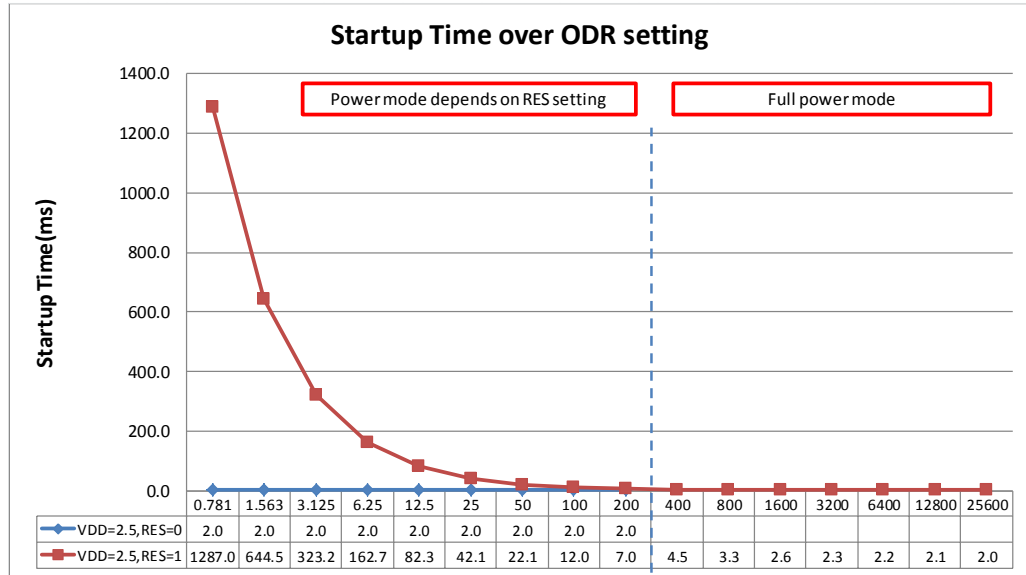
1. Current varies with Output Data Rate (ODR) as shown the chart below, and the Average Filter Control settings and can be tested using Kionix FlexSet™ Performance Optimization Tool found at <http://www.kionix.com/flexset>.
2. For I²C communication, this assumes a minimum 1.5kΩ pull-up resistor on SCL and SDA pins.
3. Start up time is from PC1 set to valid outputs. Time varies with Output Data Rate (ODR); see chart below
4. Power up time is from VDD valid to device boot completion.
5. User selectable through I²C or SPI.
6. User selectable and dependent on ODR and RES.



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

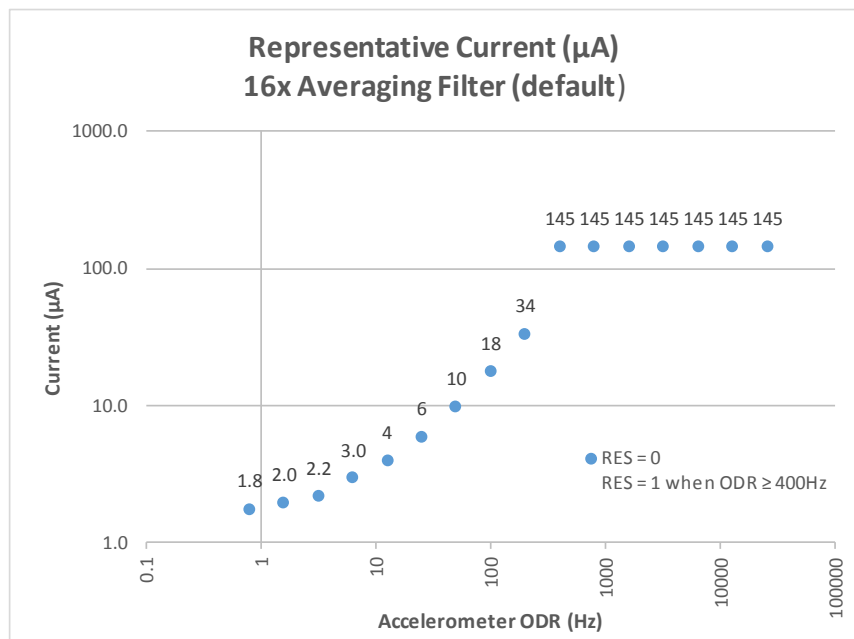
PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16


Start Up Time Profile



Current Profile

Representative Current Profile		
ODR (Hz)	RES	Current (µA)
0	Standby	0.9
0.781	0	1.8
1.563	0	2.0
3.125	0	2.2
6.25	0	3.0
12.5	0	4
25	0	6
50	0	10
100	0	18
200	0	34
400	1	145
800	1	145
1600	1	145
3200	1	145
6400	1	145
12800	1	145
25600	1	145



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Power-On Procedure

Proper functioning of power-on reset (POR) is dependent on the specific **VDD**, **VDD_{Low}**, **T_{VDD}** (rise time), and **T_{VDD_OFF}** profile of individual applications. It is recommended to minimize **VDD_{Low}**, and **T_{VDD}**, and maximize **T_{VDD_OFF}**. It is also advised that the **VDD** ramp up time **T_{VDD}** be monotonic. Note that the outputs will not be stable until **VDD** has reached its final value.

- ! *To assure proper POR, the application should be evaluated over the customer specified range of VDD, VDD_{Low}, T_{VDD}, T_{VDD_OFF} and temperature as POR performance can vary depending on these parameters.*

Please refer to Technical Note [TN004 KX1xx, KX2xx Accelerometer Power-On Procedure](#) for more information.

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Absolute Limits	V	-0.5	-	3.60
Operating Temperature Range		°C	-40	-	85
Storage Temperature Range		°C	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000

Table 3: Environmental Specifications



Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.



These products conform to RoHS Directive 2011/65/EU of the European Parliament and of the Council of the European Union that was issued June 8, 2011. Specifically, these products do not contain any non-exempted amounts of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials.

Homogenous materials are “of uniform composition throughout”. The MCV for lead, mercury, hexavalent chromium, PBB, and PBDE is 0.10%. The MCV for cadmium is 0.010%.

Applicable Exemption: 7C-I - *Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors (piezoelectronic devices) or in a glass or ceramic matrix compound.*




These products are also in conformance with REACH Regulation No 1907/2006 of the European Parliament and of the Council that was issued Dec. 30, 2011. They do not contain any Substances of Very High Concern (SVHC-161) as identified by the European Chemicals Agency as of 17 December 2014.



This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations are available upon request or from www.kionix.com.

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

Terminology

g

A unit of acceleration equal to the acceleration of gravity at the earth's surface.

$$1g = 9.8 \frac{m}{s^2}$$

One thousandth of a g (0.0098 m/ s²) is referred to as 1 milli-g (1 mg).

Sensitivity

The sensitivity of an accelerometer is the change in output per unit of input acceleration at nominal VDD and temperature. The term is essentially the gain of the sensor expressed in counts per g (counts/g) or LSB's per g (LSB/g). Occasionally, sensitivity is expressed as a resolution, i.e. milli-g per LSB (mg/LSB) or milli-g per count (mg/count). Sensitivity for a given axis is determined by measurements of the formula:

$$Sensitivity = \frac{(Output @ +1g - Output @ -1g)}{2g}$$


The sensitivity tolerance describes the range of sensitivities that can be expected from a large population of sensors at room temperature and over life. When the temperature deviates from room temperature (25°C), the sensitivity will vary by the amount shown in Table 1.

Zero-g offset

Zero-g offset or 0-g offset describes the actual output of the accelerometer when no acceleration is applied. Ideally, the output would always be in the middle of the dynamic range of the sensor (content of the OUTX, OUTY, OUTZ registers = 00h, expressed as a 2's complement number). However, because of mismatches in the sensor, calibration errors, and mechanical stress, the output can deviate from 00h. This deviation from the ideal value is called 0-g offset. The zero-g offset tolerance describes the range of 0-g offsets of a population of sensors over the operating temperature range.

Self-test

Self-test allows a functional test of the sensor without applying a physical acceleration to it. When activated, an electrostatic force is applied to the sensor, simulating an input acceleration. The sensor outputs respond accordingly. If the output signals change within the amplitude specified in Table 1, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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Functionality

Sense element

The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. This process technology allows Kionix to create mechanical silicon structures which are essentially mass-spring systems that move in the direction of the applied acceleration. Acceleration sensing is based on the principle of a differential capacitance arising from the acceleration-induced motion. Capacitive plates on the moving mass move relative to fixed capacitive plates anchored to the substrate. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit.

ASIC interface

A separate ASIC device packaged with the sense element provides all of the signal conditioning and communication with the sensor. The complete measurement chain is composed by a low-noise capacitance to voltage amplifier which converts the differential capacitance of the MEMS sensor into an analog voltage that is sent through an analog-to-digital converter. The acceleration data may be accessed through the I²C digital communications provided by the ASIC. In addition, the ASIC contains all of the logic to allow the user to choose data rates, g-ranges, filter settings, and interrupt logic. Plus, there are two programmable state machines which allow the user to create unique embedded functions based on changes in acceleration.

Factory calibration

Kionix trims the offset and sensitivity of each accelerometer by adjusting gain (sensitivity) and 0-g offset trim codes stored in non-volatile memory (OTP). Additionally, all functional register default values are also programmed into the non-volatile memory. Every time the device is turned on or a software reset command is issued, the trimming parameters and default register values are downloaded into the volatile registers to be used during active operation. This allows the device to function without further calibration.

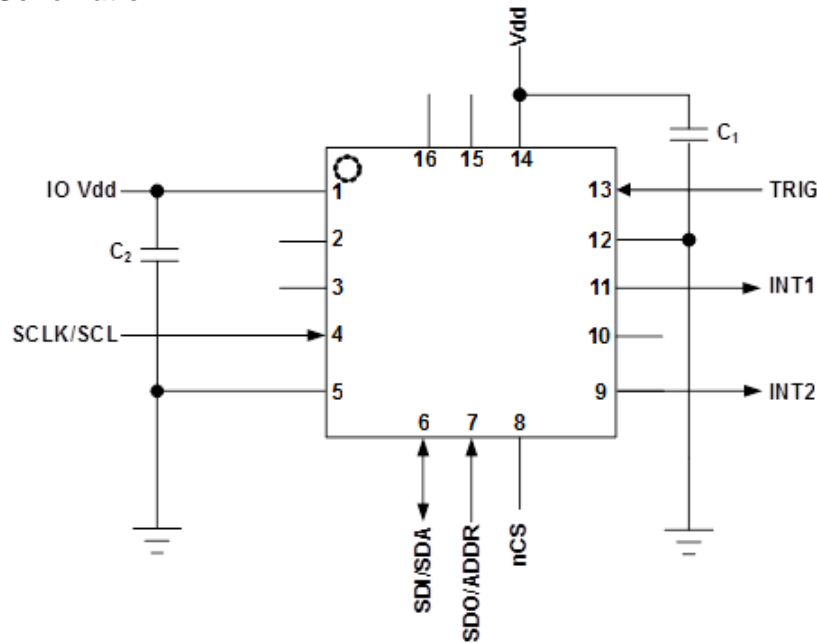


± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

Application Schematic and Pin Description

Application Schematic



Pin Descriptions

Pin	Name	Description
1	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor.
2	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating
3	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating
4	SCLK/SCL	SPI and I ² C Serial Clock
5	GND	Ground
6	SDI/SDA	SPI Data input / I2C Serial Data
7	SDO/ADDR	Serial Data Out pin during 4 wire SPI communication and part of the device address during I2C communication.
8	nCS	SPI enable / I2C mode select. Connect to GND for SPI enabled, I2C communication disabled. Connect to IO_VDD for SPI disabled, I2C communication enabled. Do not leave floating.
9	INT2	Physical Interrupt 2. Leave floating if not used.
10	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating
11	INT1	Physical Interrupt 1. Leave floating if not used.
12	GND	Ground
13	TRIG	Trigger pin for FIFO buffer control – Connect to GND when not using external trigger option.
14	VDD	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.
15	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating
16	NC	Not Internally Connected – Can be connected to VDD, IO_VDD, GND or leave floating

Table 4: Pin Description



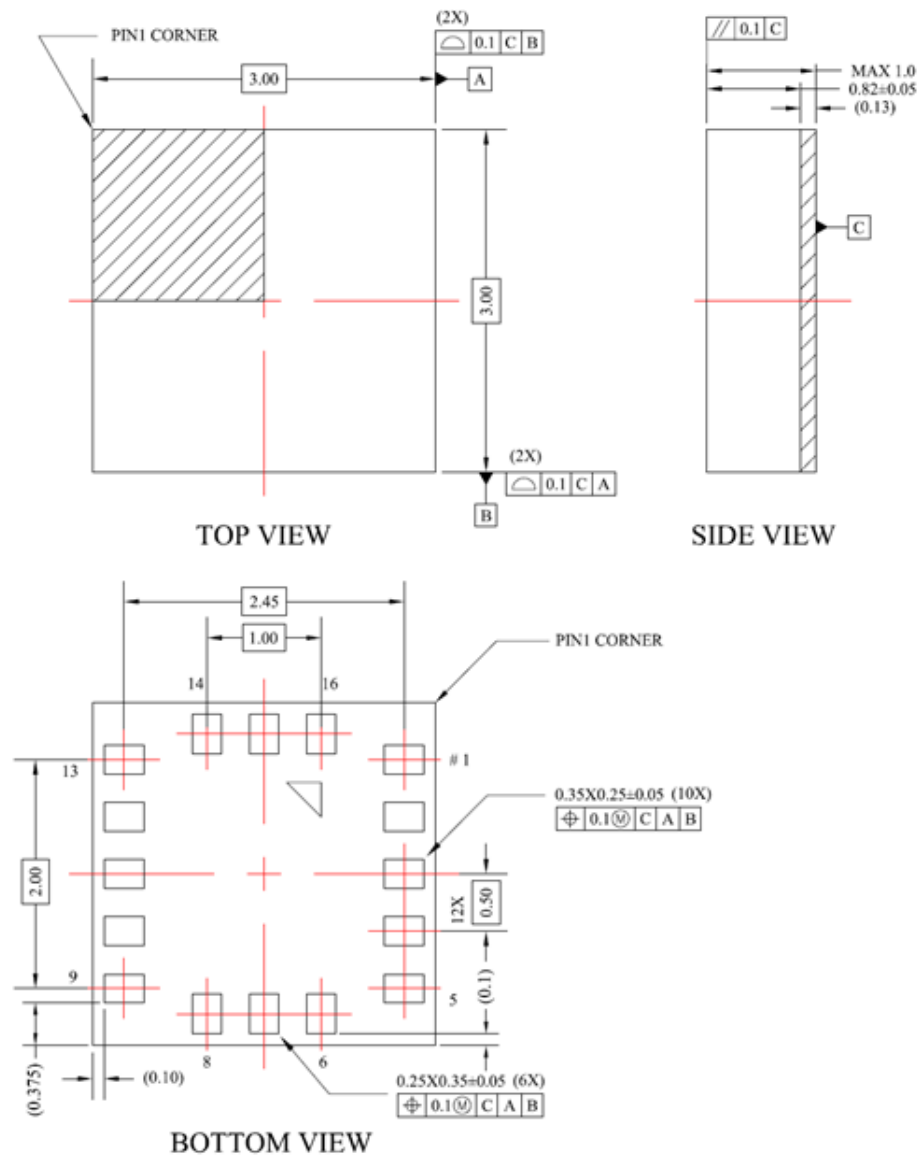
± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

Package Dimensions and Orientation

Dimensions

3 x 3 x 0.9 mm LGA



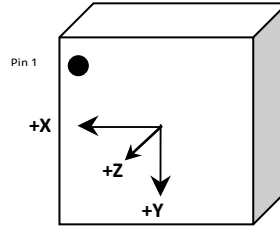
All dimensions and tolerances conform to ASME Y14.5M-1994



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

Orientation

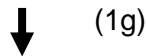


When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=0 (± 8g)

Position	1		2		3		4		5		6	
Diagram									Top 		Bottom 	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	0	0	-4096	-16	0	0	4096	16	0	0	0	0
Y (counts)	-4096	-16	0	0	4096	16	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	4096	16	-4096	-16
X-Polarity	0		-		0		+		0		0	
Y-Polarity	-		0		+		0		0		0	
Z-Polarity	0		0		0		0		+		-	



Earth's Surface



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=1 (± 16g)

Position	1		2		3		4		5		6	
Diagram									Top 		Bottom 	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	0	0	-2048	-8	0	0	2048	8	0	0	0	0
Y (counts)	-2048	-8	0	0	2048	8	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	2048	8	-2048	-8
X-Polarity	0		-		0		+		0		0	
Y-Polarity	-		0		+		0		0		0	
Z-Polarity	0		0		0		0		+		-	

↓ (1g)

Earth's Surface


Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=1, GSEL0=0 (± 32g)

Position	1		2		3		4		5		6	
Diagram									Top 		Bottom 	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	0	0	-1024	-4	0	0	1024	4	0	0	0	0
Y (counts)	-1024	-4	0	0	1024	4	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	1024	4	-1024	-4
X-Polarity	0		-		0		+		0		0	
Y-Polarity	-		0		+		0		0		0	
Z-Polarity	0		0		0		0		+		-	

↓ (1g)

Earth's Surface

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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Digital Interface

The Kionix KX224 digital accelerometer has the ability to communicate via the I²C and SPI digital serial interface protocols. This allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in Table 5 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 5: Serial Interface Terminologies

I²C Serial Interface

As previously mentioned, the KX224 accelerometer has the ability to communicate on an I²C bus. I²C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The Master, typically a micro controller, provides the serial clock signal and addresses Slave devices on the bus. The KX224 always operates as a Slave device during standard Master-Slave I²C operation.

I²C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I²C bus is considered free when both lines are high.

The I²C interface is compliant with high-speed mode, fast mode and standard mode I²C protocols.

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data ‘1’ from the Slave or transmitting data ‘0’ to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally stored address. If they match, the device considers itself addressed by the Master. The KX224 Slave Address is comprised of a user programmable part, a factory programmable part, and a fixed part, which allows for connection of multiple accelerometers to the same I²C bus. The Slave Address associated with the KX224 is 00111YX, where the user programmable bit X, is determined by the assignment of ADDR (pin 1) to GND or IO_VDD. Also, the factory programmable bit Y is set at the factory. **For KX224-1053, the factory programmable bit Y is fixed to 1** (contact your Kionix sales representative for list of available devices). Table 6 lists possible I²C addresses for KX224-1053. As a result, up to four accelerometers can be implemented on a shared I²C bus as shown in Figure 1 on the next page (e.g. two KX224-1053 accelerometers and two other accelerometers with factory programmable bit Y set to 0).

Description	Address Pad	7 bit Address	Address	<7>	<6>	<5>	<4>	<3>	Y	X	<0>
									<2>	<1>	
I2C Wr	IO_VDD	0x1F	0x3E	0	0	1	1	1	1	1	0
I2C Rd	IO_VDD	0x1F	0x3F	0	0	1	1	1	1	1	1
I2C Wr	GND	0x1E	0x3C	0	0	1	1	1	1	0	0
I2C Rd	GND	0x1E	0x3D	0	0	1	1	1	1	0	1

Table 6: I²C Slave Addresses for KX224-1053

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I²C bus is now free. Note that if the accelerometer is accessed through I²C protocol before the startup is finished a NACK signal is sent.



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

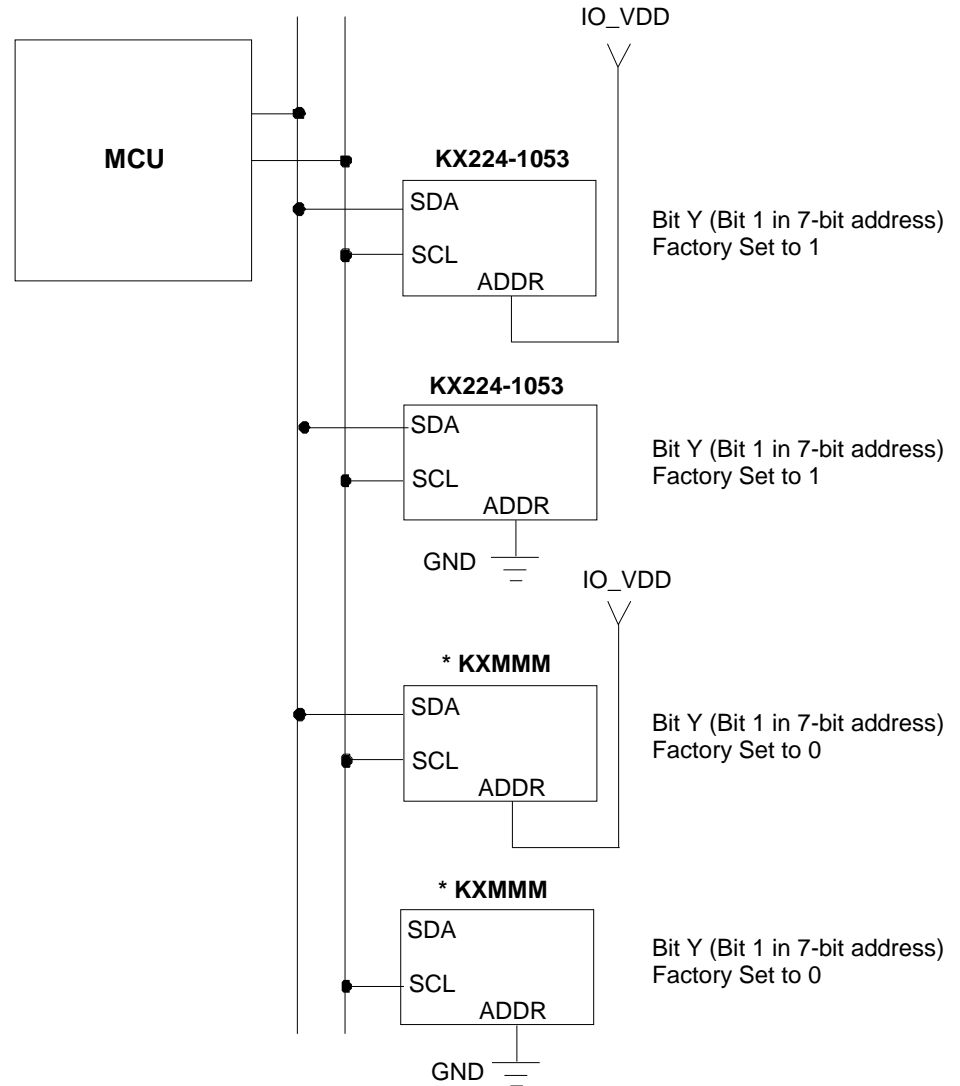



Figure 1: Multiple KX224 Accelerometers on a Shared I²C Bus

* KXMMM – contact Kionix sales representative for list of compatible devices

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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Writing to accelerometer's 8-bit Register


Upon power up, the Master must write to the KX224 accelerometer's control registers to set its operational mode. Therefore, when writing to a control register on the I²C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the accelerometer's ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the accelerometer to which 8-bit register the Master will be writing the data. Since this is I²C mode, the MSB of the RA command should always be zero (0). The accelerometer acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The accelerometer acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the accelerometer is now stored in the appropriate register. The accelerometer automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.

Note** If a STOP condition is sent on the least significant bit of write data or the following master acknowledge cycle, the last write operation is not guaranteed and it may alter the content of the affected registers

Reading from accelerometer's 8-bit Register

When reading data from a KX224 accelerometer's 8-bit register on the I²C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The accelerometer acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The accelerometer again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the accelerometer with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. The accelerometer automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page. Reading data from a buffer read register is a special case because if register address (RA) is set to buffer read register (BUF_READ) in Sequence 4, the register auto-increment feature is automatically disabled. Instead, the Read Pointer will increment to the next data in the buffer, thus allowing reading multiple bytes of data from the buffer using a single SAD+R command.

Note** Accelerometer's output data should be read in a single transaction using the auto-increment feature to prevent output data from being updated prior to intended completion of the read transaction.

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I²C bus and how the Master and Slave interact during these transfers. Table 7 defines the I²C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 7: I²C Terms

Sequence 1: The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2: The Master is writing multiple bytes to the Slave.


Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3: The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4: The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5: HS-mode data transfer of the Master writing multiple bytes to the Slave.

Speed	FS-mode			HS-mode							FS-mode	
Master	S	M-code	NACK	Sr	SAD + W		RA		DATA		P	
Slave						ACK		ACK		ACK		

n bytes + ack.

Sequence 6: HS-mode data transfer of the Master receiving multiple bytes of data from the Slave.

Speed	FS-mode			HS-mode			
Master	S	M-code	NACK	Sr	SAD + W		RA
Slave						ACK	ACK

Speed	HS-mode							FS-mode
Master	Sr	SAD + R					NACK	P
Slave			ACK	DATA	ACK	DATA		

(n-1) bytes + ack.



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

I²C Timing Diagram

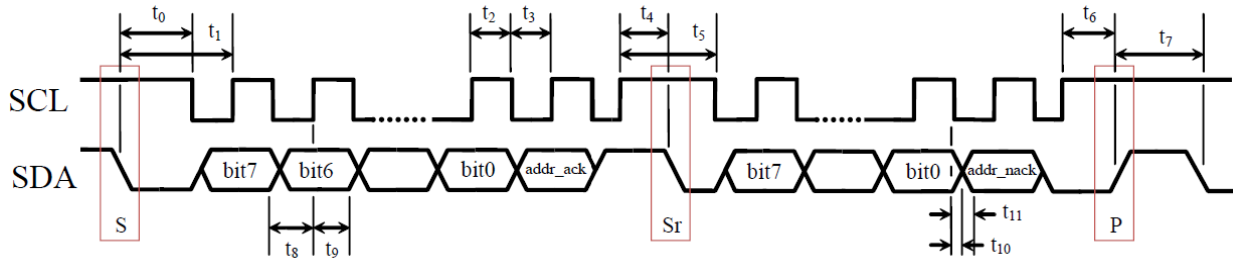



Table 8: I²C Timing (Fast Mode)

Number	Description	MIN	MAX	Units
t ₀	SDA low to SCL low transition (Start event)	50	-	ns
t ₁	SDA low to first SCL rising edge	100	-	ns
t ₂	SCL pulse width: high	100	-	ns
t ₃	SCL pulse width: low	100	-	ns
t ₄	SCL high before SDA falling edge (Start Repeated)	50	-	ns
t ₅	SCL pulse width: high during a S/Sr/P event	100	-	ns
t ₆	SCL high before SDA rising edge (Stop)	50	-	ns
t ₇	SDA pulse width: high	25	-	ns
t ₈	SDA valid to SCL rising edge	50	-	ns
t ₉	SCL rising edge to SDA invalid	50	-	ns
t ₁₀	SCL falling edge to SDA valid (when slave is transmitting)	-	100	ns
t ₁₁	SCL falling edge to SDA invalid (when slave is transmitting)	0	-	ns
Note	Recommended I ² C CLK	2.5	-	us

	<p align="center">± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications</p>	<p>PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16</p>
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SPI Communications

4-Wire SPI Interface

The KX224 also utilize an integrated 4-Wire Serial Peripheral Interface (SPI) for digital communication. The SPI interface is primarily used for synchronous serial communication between one Master device and one or more Slave devices. The Master, typically a micro controller, provides the SPI clock signal (SCLK) and determines the state of Chip Select (nCS). The accelerometer always operates as a Slave device during standard Master-Slave SPI operation.

4-wire SPI is a synchronous serial interface that uses two control and two data lines. With respect to the Master, the Serial Clock output (SCLK), the Data Output (SDI or MOSI) and the Data Input (SDO or MISO) are shared among the Slave devices. The Master generates an independent Chip Select (nCS) for each Slave device that goes low at the start of transmission and goes back high at the end. The Slave Data Output (SDO) line, remains in a high-impedance (hi-z) state when the device is not selected, so it does not interfere with any active devices. This allows multiple Slave devices to share a master SPI port as shown in Figure 2 below.

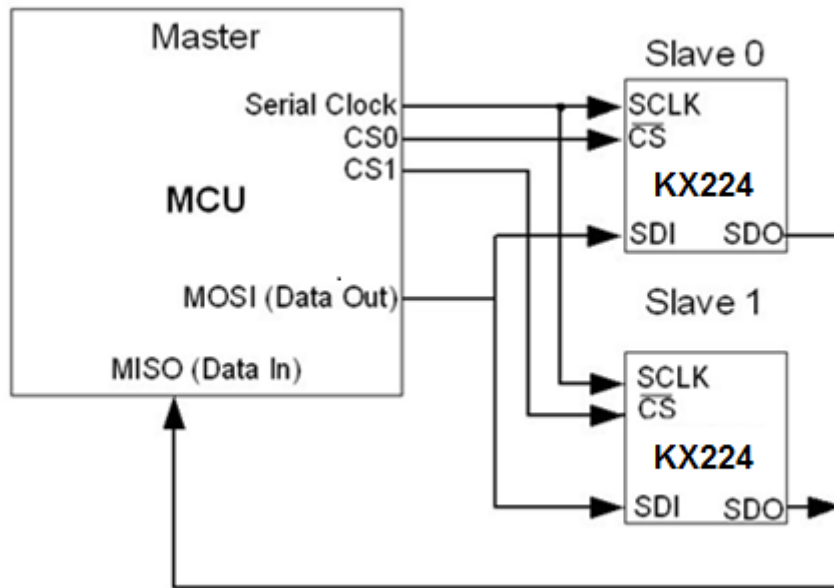


Figure 2: 4-wire SPI Connections



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

4-Wire SPI Timing Diagram

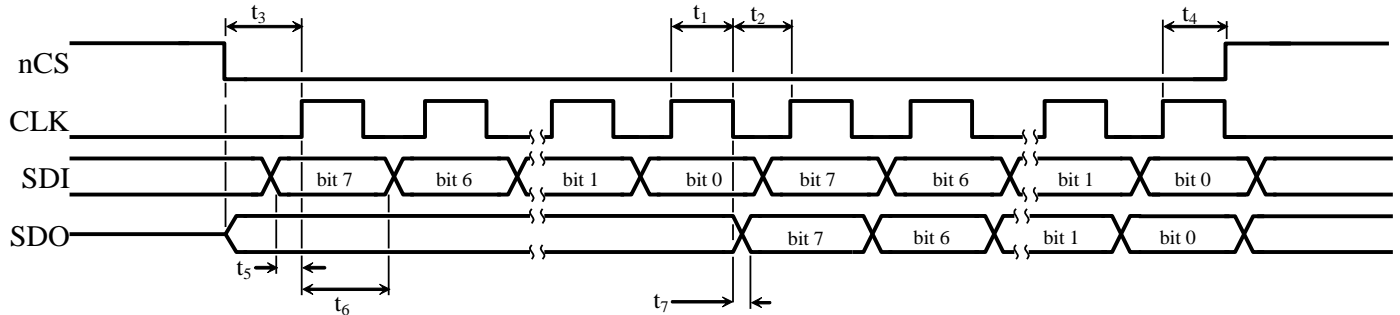


Table 9: 4-Wire SPI Timing

Number	Description	MIN	MAX	Units
t_1	CLK pulse width: high	40		ns
t_2	CLK pulse width: low	40		ns
t_3	nCS low to first CLK rising edge	20		ns
t_4	nCS low after the final CLK rising edge	30		ns
t_5	SDI valid to CLK rising edge	10		ns
t_6	CLK rising edge to SDI invalid	10		ns
t_7	CLK falling edge to SDO valid		35	ns

Notes

- t_7 is only present during reads.
- Timings are for VDD of 1.8V to 3.6V with 1k Ω pull-up resistor and maximum 20pF load capacitor on SDO.



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

4-Wire Read and Write Registers

The registers embedded in the KX224 accelerometer have 8-bit addresses. Upon power up, the Master must write to the accelerometer's control registers to set its operational mode. On the falling edge of nCS, a 2-byte command is written to the appropriate control register. The first byte initiates the write to the appropriate register, and is followed by the user-defined, data byte. The MSB (Most Significant Bit) of the register address byte will indicate "0" when writing to the register and "1" when reading from the register. This operation occurs over 16 clock cycles. All commands are sent MSB first. The host must return nCS high for at least one clock cycle before the next data request. However, when data is being read from a buffer read register (BUF_READ), the nCS signal can remain low until the buffer is read. Figure 3 below shows the timing diagram for carrying out an 8-bit register write operation.

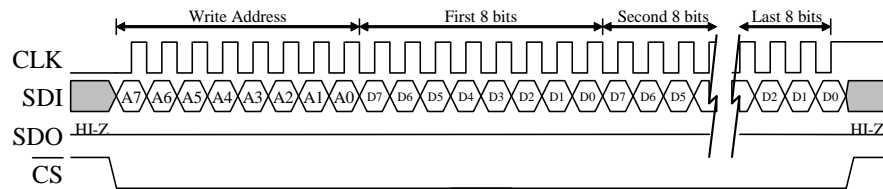


Figure 3: Timing Diagram for 8-Bit Register Write Operation

In order to read an 8-bit register, an 8-bit register address must be written to the accelerometer to initiate the read. The MSB of this register address byte will indicate "0" when writing to the register and "1" when reading from the register. Upon receiving the address, the accelerometer returns the 8-bit data stored in the addressed register. This operation also occurs over 16 clock cycles. All returned data is sent MSB first, and the host must return nCS high for at least one clock cycle before the next data request. Figure 4 shows the timing diagram for an 8-bit register read operation.

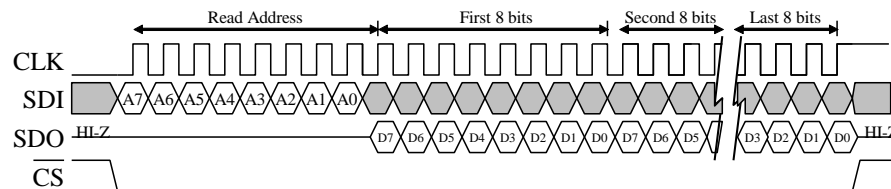


Figure 4: Timing Diagram for 8-Bit Register Read Operation



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

3-Wire SPI Interface

The KX224 also utilize an integrated 3-Wire Serial Peripheral Interface (SPI) for digital communication. 3-wire SPI is a synchronous serial interface that uses two control lines and one data line. With respect to the Master, the Serial Clock output (SCLK), the Data Output/Input (SDI) are shared among the Slave devices. The Master generates an independent Chip Select (\bar{CS}) for each Slave device that goes low at the start of transmission and goes back high at the end. This allows multiple Slave devices to share a master SPI port as shown in Figure 5 below.

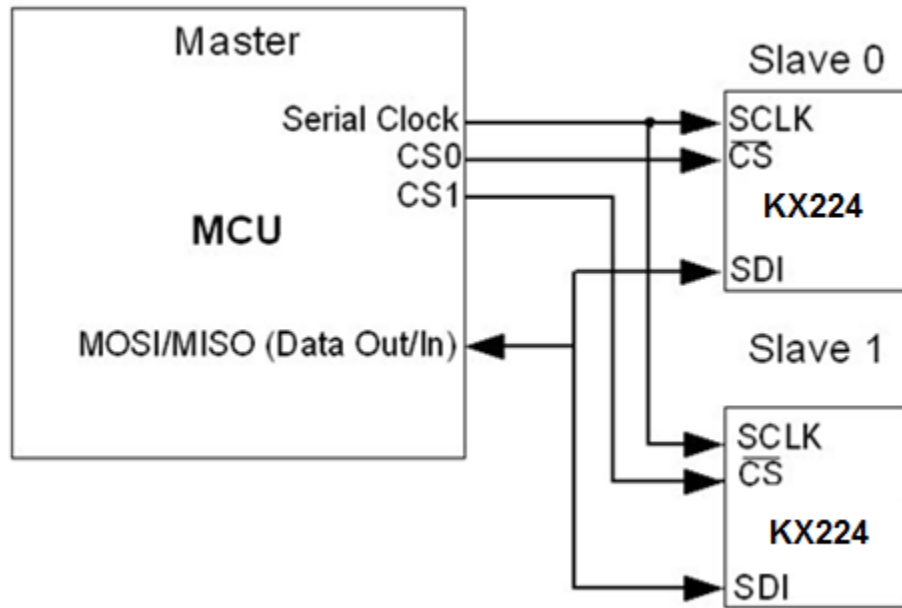


Figure 5: 3-wire SPI Connections



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

3-Wire SPI Timing Diagram

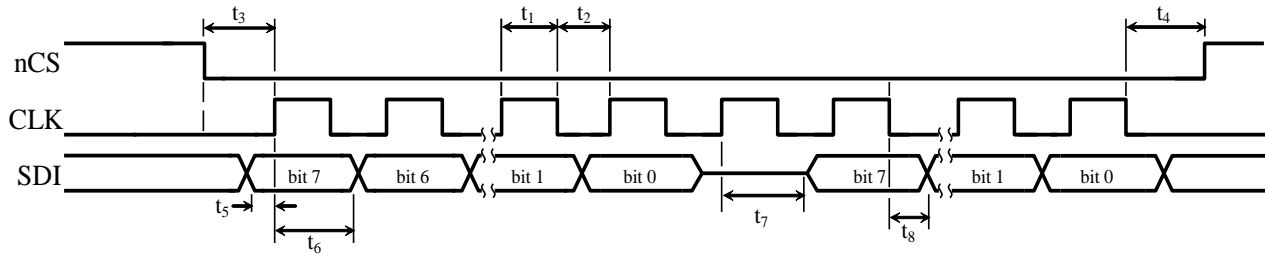



Table 10: 3-Wire SPI Timing

Number	Description	MIN	MAX	Units
t ₁	CLK pulse width: high	40	-	ns
t ₂	CLK pulse width: low	40	-	ns
t ₃	nCS low to first CLK rising edge	20	-	ns
t ₄	nCS low after the final CLK falling edge	20	-	ns
t ₅	SDI valid to CLK rising edge	10	-	ns
t ₆	CLK rising edge to SDI input invalid	10	-	ns
t ₇	CLK extra clock cycle rising edge to SDI output	-	-	ns
t ₈	CLK falling edge to SDI output becomes valid	-	35	ns

Notes

1. t₇ and t₈ are only present during reads.
2. Timings are for VDD of 1.8V to 3.6V with 1kΩ pull-up resistor and maximum 20pF load capacitor on SDI.

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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3-Wire Read and Write Registers

The registers embedded in the KX224 accelerometer have 8-bit addresses. Upon power up, the Master must write to the accelerometer’s control registers to set its operational mode. On the falling edge of nCS, a 2-byte command is written to the appropriate control register. The first byte initiates the write to the appropriate register, and is followed by the user-defined, data byte. The MSB (Most Significant Bit) of the register address byte will indicate “0” when writing to the register and “1” when reading from the register. A read operation occurs over 17 clock cycles and a write operation occurs over 16 clock cycles. All commands are sent MSB first. The host must return nCS high for at least one clock cycle before the next data request. However, when data is being read from a buffer read register (BUF_READ), the nCS signal can remain low until the buffer is read. Figure 6 below shows the timing diagram for carrying out an 8-bit register write operation.

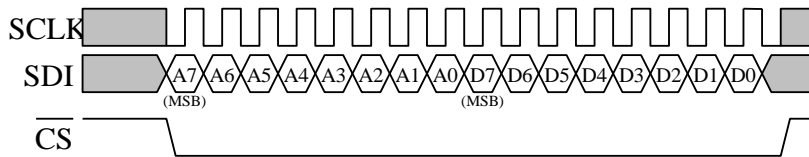


Figure 6: Timing Diagram for 8-Bit Register Write Operation

In order to read an 8-bit register, an 8-bit register address must be written to the accelerometer to initiate the read. The MSB of this register address byte will indicate “0” when writing to the register and “1” when reading from the register. Upon receiving the address, the accelerometer returns the 8-bit data stored in the addressed register. For 3-wire read operations, one extra clock cycle between the address byte and the data output byte is required. Therefore, this operation occurs over 17 clock cycles. All returned data is sent MSB first, and the host must return nCS high for at least one clock cycle before the next data request. Figure 7 shows the timing diagram for an 8-bit register read operation.

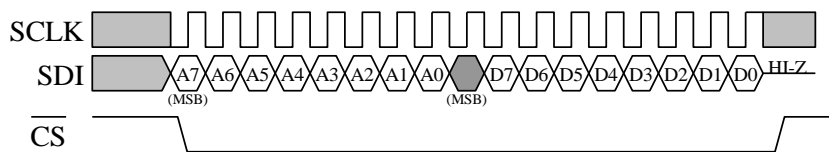


Figure 7: Timing Diagram for 8-Bit Register Read Operation



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

Embedded Registers

The KX224 accelerometer has 57 embedded 8-bit registers that are accessible by the user. This section contains the addresses for all embedded registers and also describes bit functions of each register. Table 11 below provides a listing of the accessible 8-bit registers and their addresses.

Address	Register Name	R/W	Address	Register Name	R/W
00h	XHPL	R	21h	INC6*	R/W
01h	XPH	R	22h	TILT_TIMER*	R/W
02h	YHPL	R	23h	WUFC*	R/W
03h	YPH	R	24h	TDTRC*	R/W
04h	ZHPL	R	25h	TDTC*	R/W
05h	ZPH	R	26h	TTH*	R/W
06h	XOUTL	R	27h	TTL*	R/W
07h	XOUTH	R	28h	FTD*	R/W
08h	YOUTL	R	29h	STD*	R/W
09h	YOUTH	R	2Ah	TLT*	R/W
0Ah	ZOUTL	R	2Bh	TWS*	R/W
0Bh	ZOUTH	R	2Ch	FFTH*	R/W
0Ch	COTR	R	2Dh	FFC*	R/W
0Dh	Kionix Reserved		2Eh	FFCNTL*	R/W
0Eh	Kionix Reserved		2Fh	Kionix Reserved	
0Fh	Who_AM_I	R/W	30h	ATH*	R/W
10h	TSCP	R	31h	Kionix Reserved	
11h	TSPP	R	32h	TILT_ANGLE_LL*	R/W
12h	INS1	R	33h	TILT_ANGLE_HL*	R/W
13h	INS2	R	34h	HYST_SET*	R/W
14h	INS3	R	35h	LP_CNTL*	R/W
15h	STAT	R	36h	Kionix Reserved	
16h	Kionix Reserved		37h	Kionix Reserved	
17h	INT_REL	R	38h	Kionix Reserved	
18h	CNTL1*	R/W	39h	Kionix Reserved	
19h	CNTL2*	R/W	3Ah	BUF_CNTL1*	R/W
1Ah	CNTL3*	R/W	3Bh	BUF_CNTL2*	R/W
1Bh	ODCNTL*	R/W	3Ch	BUF_STATUS_1	R
1Ch	INC1*	R/W	3Dh	BUF_STATUS_2	R
1Dh	INC2*	R/W	3Eh	BUF_CLEAR	W
1Eh	INC3*	R/W	3Fh	BUF_READ	R
1Fh	INC4*	R/W	60h	SELF_TEST	R/W
20h	INC5*	R/W			

* Note: - When changing the contents of these registers, the PC1 bit in CNTL1 must first be set to "0".
 - Reserved registers should not be written.

Table 11: Register Map

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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Register Descriptions

Accelerometer Outputs

These registers contain up to 16-bits of valid acceleration data for each axis. Depending on the setting of the RES bit in CNTL1, the user may choose to read only the 8 MSB thus reading an effective 8-bit resolution. When BRES = 0 in BUF_CNTL2 the 8 MSB is the only data recorded in the buffer. The data is updated every user-defined ODR period, is protected from overwrite during each read, and can be converted from digital counts to acceleration (g) per Table 12 below. The register acceleration output binary data is represented in 2's complement format. For example, if N = 16 bits, then the Counts range is from -32768 to 32767, and if N = 8 bits, then the Counts range is from -128 to 127.

16-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = ±8g	Range = ±16g	Range = ±32g
0111 1111 1111 1111	32767	+7.99966g	+15.99952g	+31.99904g
0111 1111 1111 1110	32766	+7.99952g	+15.99904g	+31.99808g
...
0000 0000 0000 0001	1	+0.00024g	+0.00048g	+0.00096g
0000 0000 0000 0000	0	0.000g	0.0000g	0.0000g
1111 1111 1111 1111	-1	-0.00024g	-0.00048g	-0.00096g
...
1000 0000 0000 0001	-32767	-7.99966g	-15.99952g	-31.99904g
1000 0000 0000 0000	-32768	-8.00000g	-16.00000g	-32.00000g

8-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = ±8g	Range = ±16g	Range = ±32g
0111 1111	127	+7.9375g	+15.875g	+31.75g
0111 1110	126	+7.8750g	+15.750g	+31.50g
...
0000 0001	1	+0.0625g	+0.125g	+0.25g
0000 0000	0	0.0000g	0.000g	0.00g
1111 1111	-1	-0.0625g	-0.125g	-0.25g
...
1000 0001	-127	-7.9375g	-15.875g	-31.75g
1000 0000	-128	-8.0000g	-16.000g	-32.00g

Table 12: Acceleration (g) Calculation



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

XHP_L

X-axis high pass filter accelerometer output least significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3.

R	R	R	R	R	R	R	R
XHPD7	XHPD6	XHPD5	XHPD4	XHPD3	XHPD2	XHPD1	XHPD0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x00h							

XHP_H

X-axis high pass filter accelerometer output most significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3.

R	R	R	R	R	R	R	R
XHPD15	XHPD14	XHPD13	XHPD12	XHPD11	XHPD10	XHPD9	XHPD8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x01h							

YHP_L


Y-axis high pass filter accelerometer output least significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3.

R	R	R	R	R	R	R	R
YHPD7	YHPD6	YHPD5	YHPD4	YHPD3	YHPD2	YHPD1	YHPD0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x02h							

YHP_H

Y-axis high pass filter accelerometer output most significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3.

R	R	R	R	R	R	R	R
YHPD15	YHPD14	YHPD13	YHPD12	YHPD11	YHPD10	YHPD9	YHPD8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x03h							

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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ZHP_L

Z-axis high pass filter accelerometer output least significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3

R	R	R	R	R	R	R	R
ZHPD7	ZHPD6	ZHPD5	ZHPD4	ZHPD3	ZHPD2	ZHPD1	ZHPD0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x04h							

ZHP_H

Z-axis high pass filter accelerometer output most significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3.

R	R	R	R	R	R	R	R
ZHPD15	ZHPD14	ZHPD13	ZHPD12	ZHPD11	ZHPD10	ZHPD9	ZHPD8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x05h							

XOUT_L

X-axis accelerometer output least significant byte. Data is updated at the ODR frequency determined by OSA in ODCNTL.

R	R	R	R	R	R	R	R
XOUTD7	XOUTD6	XOUTD5	XOUTD4	XOUTD3	XOUTD2	XOUTD1	XOUTD0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x06h							

XOUT_H

X-axis accelerometer output most significant byte. Data is updated at the ODR frequency determined by OSA in ODCNTL.

R	R	R	R	R	R	R	R
XOUTD15	XOUTD14	XOUTD13	XOUTD12	XOUTD11	XOUTD10	XOUTD9	XOUTD8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x07h							



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

YOUT_L

Y-axis accelerometer output least significant byte. Data is updated at the ODR frequency determined by OSA in ODCNTL.

R	R	R	R	R	R	R	R
YOUTD7	YOUTD6	YOUTD5	YOUTD4	YOUTD3	YOUTD2	YOUTD1	YOUTD0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x08h							

YOUT_H

Y-axis accelerometer output most significant byte. Data is updated at the ODR frequency determined by OSA in ODCNTL.

R	R	R	R	R	R	R	R
YOUTD15	YOUTD14	YOUTD13	YOUTD12	YOUTD11	YOUTD10	YOUTD9	YOUTD8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x09h							

ZOUT_L


Z-axis accelerometer output least significant byte. Data is updated at the ODR frequency determined by OSA in ODCNTL.

R	R	R	R	R	R	R	R
ZOUTD7	ZOUTD6	ZOUTD5	ZOUTD4	ZOUTD3	ZOUTD2	ZOUTD1	ZOUTD0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x0Ah							

ZOUT_H

Z-axis accelerometer output most significant byte. Data is updated at the ODR frequency determined by OSA in ODCNTL.

R	R	R	R	R	R	R	R
YOUTD15	YOUTD14	YOUTD13	YOUTD12	YOUTD11	YOUTD10	YOUTD9	YOUTD8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x0Bh							

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

COTR

This register can be used to verify proper integrated circuit functionality. It always has a byte value of 0x55h unless the COTC bit in CNTL2 is set. At that point this value is set to 0xAAh. The byte value is returned to 0x55h after reading this register and the COTC bit in CNTL2 is cleared.

R	R	R	R	R	R	R	R	
DCSTR7	DCSTR6	DCSTR5	DCSTR4	DCSTR3	DCSTR2	DCSTR1	DCSTR0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01010101
I ² C Address: 0x0Ch								

WHO_AM_I

This register can be used for supplier recognition, as it can be factory written to a known byte value. The default value is 0x2Bh.

R	R	R	R	R	R	R	R	
WIA7	WIA6	WIA5	WIA4	WIA3	WIA2	WIA1	WIA0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00101011
I ² C Address: 0x0Fh								


Tilt Position Registers

These two registers report previous and current position data that is updated at the user-defined ODR frequency and is protected during register read. Table 13 describes the reported position for each bit value.

TSCP

Current Tilt Position Register.

R	R	R	R	R	R	R	R	
0	0	LE	RI	DO	UP	FD	FU	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00100000
I ² C Address: 0x10h								

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

TSPP

Previous Tilt Position Register.

R	R	R	R	R	R	R	R	
0	0	LE	RI	DO	UP	FD	FU	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00100000
I ² C Address: 0x11h								

Bit	Description
LE	Left State (X-)
RI	Right State (X+)
DO	Down State (Y-)
UP	Up State (Y+)
FD	Face-Down State (Z-)
FU	Face-Up State (Z+)

Table 13: Tilt Position

Interrupt Source Registers

These three registers report interrupt state changes. This data is updated when a new interrupt event occurs and each application's result is latched until the interrupt release register is read.

INS1

This register indicates the triggering axis when a tap/double tap interrupt occurs. Data is updated at the ODR settings determined by OTDT<2:0> in CNTL3.

R	R	R	R	R	R	R	R	
0	0	TLE	TRI	TDO	TUP	TFD	TFU	
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
I ² C Address: 0x12h								



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

Bit	Description
TLE	X Negative (X-) Reported
TRI	X Positive (X+) Reported
TDO	Y Negative (Y-) Reported
TUP	Y Positive (Y+) Reported
TFD	Z Negative (Z-) Reported
TFU	Z Positive (Z+) Reported

Table 14: Directional Tap™ Reporting

INS2

This Register tells witch function caused an interrupt.


R	R	R	R	R	R	R	R
FFS	BFI	WMI	DRDY	TDTS1	TDTS0	WUFS	TPS
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x13h							

FFS – Free fall. This bit is cleared when the interrupt latch release register (INT_REL) is read.
 FFS = 0 – No Free fall
 FFS = 1 – Free fall has activated the interrupt

BFI – indicates buffer full interrupt. Automatically cleared when at least one sample is read from the buffer or following the write to BUF_CLEAR register.
 BFI = 0 – Buffer is not full
 BFI = 1 – Buffer is full

WMI – Watermark interrupt, bit is set to 1 when FIFO has filled up to the value stored in the sample bits. This bit is automatically cleared when FIFO/FILO is read and the content returns to a value below the value stored in the sample bits, or following the write to BUF_CLEAR register.
 WMI = 0 – Buffer watermark has not been exceeded
 WMI = 1 – Buffer watermark has been exceeded

DRDY – indicates that new acceleration data (0x06h to 0x0Bh) is available. This bit is cleared when acceleration data is read or the interrupt release register INT_REL is read.
 DRDY = 0 – new acceleration data not available
 DRDY = 1 - new acceleration data available

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

TDTS(1,0) – status of tap/double tap, bit is released when interrupt release register INT_REL is read.

TDTS1	TDTS0	Event
0	0	No Tap
0	1	Single Tap
1	0	Double Tap
1	1	Do not exist

WUFS – Status of Wake up. This bit is cleared when the interrupt release register INT_REL is read.

WUFS = 1 – Motion has activated the interrupt

WUFS = 0 – No motion

TPS – Tilt Position status. This bit is cleared when the interrupt release register INT_REL is read.

TPS = 0 – Position not changed

TPS = 1 – Position changed

INS3

This register reports the axis and direction of detected motion.

R	R	R	R	R	R	R	R
0	0	XNWU	XPWU	YNWU	YPWU	ZNWU	ZPWU
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x14h							

Bit	Description
XNWU	X Negative (X-) Reported
XPWU	X Positive (X+) Reported
YNWU	Y Negative (Y-) Reported
YPWU	Y Positive (Y+) Reported
ZNWU	Z Negative (Z-) Reported
ZPWU	Z Positive (Z+) Reported

Table 15: Motion Detection™ Reporting

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

STATUS_REG

This register reports the status of the interrupt.

R	R	R	R	R	R	R	R
0	0	0	INT	0	0	0	0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x15h							

INT reports the combined (OR) interrupt information of all features. When BFI and WMI in INS2 are 0, the INT bit is released to 0 when INT_REL is read. If WMI or BFI is 1, INT bit remains at 1 until they are cleared by FIFO/FILO buffer read.

0 = no interrupt event

1 = interrupt event has occurred

INT_REL

Latched interrupt source information (INS1, INS2, INS3 except WMI/BFI and INT when WMI/BFI is zero) is cleared and physical interrupt latched pin is changed to its inactive state when this register is read. Read value is dummy.

R	R	R	R	R	R	R	R
X	X	X	X	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x17h							

CNTL1

Read/write control register that controls the main feature set.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PC1	RES	DRDYE	GSEL1	GSEL0	TDTE	WUFE	TPE	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x18h								

PC1 controls the operating mode of the KX224. Please allow 1.5/ODR delay time when transitioning from stand-by PC1 = 0 to operating mode PC1 = 1 to allow new settings to load.


0 = stand-by mode

1 = operating mode

RES determines the performance mode of the KX224. The noise varies with ODR, RES and different LP_CNTL settings possibly reducing the effective resolution. Note that to change the value of this bit, the PC1 bit must first be set to "0".

0 = low current.

1 = high resolution.

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

DRDYE enables the reporting of the availability of new acceleration data as an interrupt. Note that to change the value of this bit, the PC1 bit must first be set to “0”.
0 = availability of new acceleration data is not reflected as an interrupt
1 = availability of new acceleration data is reflected as an interrupt

GSEL1, GSEL0 selects the acceleration range of the accelerometer outputs per Table 16. Note that to change the value of this bit, the PC1 bit must first be set to “0”.

GSEL1	GSEL0	Range
0	0	±8g
0	1	±16g
1	0	±32g

Table 16: Selected Acceleration Range

TDTE enables the Directional Tap™ function that will detect single and double tap events. Note that to change the value of this bit, the PC1 bit must first be set to “0”.
TDTE = 0 – disable
TDTE = 1 – enable

WUFE enables the Wake Up (motion detect) function. 0= disabled, 1= enabled. Note that to change the value of this bit, the PC1 bit must first be set to “0”.
0 = Wake Up function disabled
1 = Wake Up function enabled

TPE enables the Tilt Position function that will detect changes in device orientation. Note that to change the value of this bit, the PC1 bit must first be set to “0”.
TPE = 0 – disable
TPE = 1 – enable

CNTL2

Read/write control register that provides more feature set control. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SRST	COTC	LEM	RIM	DOM	UPM	FDM	FUM	00111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
I ² C Address: 0x19h								



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

SRST initiates software reset, which performs the RAM reboot routine. This bit will remain 1 until the RAM reboot routine is finished.

SRST = 0 – no action

SRST = 1 – start RAM reboot routine

COTC Command test control.

COTC = 0 – no action

COTC = 1 – sets COTR register to 0xAAh and when COTR is read, sets this bit to 0 and sets COTR to 0x55h

LEM, RIM, DOM, UPM, FDM, FUM these bits control the tilt axis mask. Per Table 17, if a direction's bit is set to one (1), tilt in that direction will generate an interrupt. If it is set to zero (0), tilt in that direction will not generate an interrupt. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to "0".

Bit	Description
LEM	X Negative (X-)
RIM	X Positive (X+)
DOM	Y Negative (Y-)
UPM	Y Positive (Y+)
FDM	Z Negative (Z-)
FUM	Z Positive (Z+)

Table 17: Tilt Direction™ Axis Mask

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

CNTL3

This control register sets the output data rates for Tilt, Directional Tap™, and the Motion Wake Up digital engines. The output data rate set in this register and the averaging filter control settings set in LP_CNTL register, will have an effect on overall performance of the digital engines and the power consumption of the accelerometer. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
OTP1	OTP0	OTDT2	OTDT1	OTDT0	OWUF2	OWUF1	OWUF0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	10011000
I ² C Address: 0x1Ah								

OTP1, OTP0 sets the output data rate for the Tilt Position function per Table 18. The default Tilt Position ODR is 12.5Hz.

OTP1	OTP0	Output Data Rate
0	0	1.563Hz
0	1	6.25Hz
1	0	12.5Hz
1	1	50Hz

Table 18: Tilt Position Function Output Data Rate

OTDT2, OTDT1, OTDT0 sets the output data rate for the Directional Tap™ function per Table 19. The default Directional Tap™ ODR is 400Hz.

OTDT2	OTDT1	OTDT0	Output Data Rate
0	0	0	50Hz
0	0	1	100Hz
0	1	0	200Hz
0	1	1	400Hz
1	0	0	12.5Hz
1	0	1	25Hz
1	1	0	800Hz
1	1	1	1600Hz

Table 19: Directional Tap™ Function Output Data Rate




± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

***OWUF2, OWUF1, OWUF0** sets the output data rate for the general motion detection function and the high-pass filtered outputs per Table 20. The default Motion Wake Up ODR is 0.781Hz.*

OWUF2	OWUF1	OWUF0	Output Data Rate
0	0	0	0.781Hz
0	0	1	1.563Hz
0	1	0	3.125Hz
0	1	1	6.250Hz
1	0	0	12.5Hz
1	0	1	25Hz
1	1	0	50Hz
1	1	1	100Hz

Table 20: Motion Wake Up Function Output Data Rate

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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ODCNTL

This register is responsible for configuring ODR (output data rate) and filter settings. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
IIR_BYPASS	LPRO	RESERVED	RESERVED	OSA3	OSA2	OSA1	OSA0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	0000010
I ² C Address: 0x1Bh								

IIR_BYPASS filter bypass mode

IIR_BYPASS = 0 – filtering applied

IIR_BYPASS = 1 – filter bypassed

LPRO low-pass filter roll off control

LPRO = 0 – filter corner frequency set to ODR/9

LPRO = 1 – filter corner frequency set to ODR/2

OSA3, OSA2, OSA1, OSA0 acceleration output data rate. The default ODR is 50Hz.


OSA3	OSA2	OSA1	OSA0	Output Data Rate
0	0	0	0	12.5Hz*
0	0	0	1	25Hz*
0	0	1	0	50Hz*
0	0	1	1	100Hz*
0	1	0	0	200Hz*
0	1	0	1	400Hz***
0	1	1	0	800Hz
0	1	1	1	1600Hz
1	0	0	0	0.781Hz*
1	0	0	1	1.563Hz*
1	0	1	0	3.125Hz*
1	0	1	1	6.25Hz*
1	1	0	0	3200Hz**
1	1	0	1	6400Hz**
1	1	1	0	12800Hz**
1	1	1	1	25600Hz**

Table 21: Accelerometer Output Data Rates (ODR)

* Low Current mode available, all other data rates will default to High Resolution mode

** If the interrupt pin is enabled and set to pulse mode, the pulse width is about 10us over 1600Hz ODR. And when ODR is up to 1600Hz, the pulse width is about 50us.

*** 400Hz High Resolution mode only (will not output in Low Current mode)

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

INC1

This register controls the settings for the physical interrupt pin INT1. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PWSEL11	PWSEL10	IEN1	IEA1	IEL1	Reserved	STPOL	SPI3E	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00010000
I ² C Address: 0x1Ch								

PWSEL1<1:0> – Pulse interrupt 1 width configuration

00 = 50us (10us if OSA > 1600Hz)

01 = 1 * OSA period

10 = 2 * OSA periods

11 = 4 * OSA periods

When *PWSEL1* > 0, Interrupt source auto-clearing (*ACLR1*=1) should be set to keep consistency between the internal status and the physical interrupt.

IEN1 enables/disables the physical interrupt pin

IEN = 0 – physical interrupt pin is disabled

IEN = 1 – physical interrupt pin is enabled

IEA1 sets the polarity of the physical interrupt pin

IEA = 0 – polarity of the physical interrupt pin is active low

IEA = 1 – polarity of the physical interrupt pin is active high

IEL1 sets the response of the physical interrupt pin

IEL = 0 – the physical interrupt pin latches until it is cleared by reading *INT_REL*

IEL = 1 – the physical interrupt pin will transmit one pulse configurable by *PWSEL1*

STPOL sets the polarity of Self Test

STPOL = 0 – Negative


STPOL = 1 – Positive

SPI3E sets the 3-wire SPI interface*

SPI3E = 0 – disabled

SPI3E = 1 – enabled

*The *SPI3E* bit should be set to 0 when I²C communication is used.

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER:
		KX224-1053
		Rev. 1.0
		26-Sep-16

INC2

This register controls which axis and direction of detected motion can cause an interrupt. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	AOI	XNWUE	XPWUE	YNWUE	YPWUE	ZNWUE	ZPWUE	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00111111
I ² C Address: 0x1Dh								

AOI – AND-OR configuration on motion detection

0 – OR combination between selected directions

1 – AND combination between selected axes

Ex. If all directions are enabled,

Active state in OR configuration = (XN || XP || YN || TP || ZN || ZP)

Active state in AND configuration = (XN || XP) && (YN || YP) && (ZN || ZP)

XNWU – x negative (x-): 0 = disabled, 1 = enabled

XPWU – x positive (x+): 0 = disabled, 1 = enabled

YNWU – y negative (y-): 0 = disabled, 1 = enabled

YPWU – y positive (y+): 0 = disabled, 1 = enabled

ZNWU – z negative (z-): 0 = disabled, 1 = enabled

ZPWU – z positive (z+): 0 = disabled, 1 = enabled

INC3

This register controls which axis and direction of tap/double tap can cause an interrupt. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	TLEM	TRIM	TDOM	TUPM	TFDM	TFUM	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00111111
I ² C Address: 0x1Eh								

TLEM – x negative (x-): 0 = disabled, 1 = enabled


TRIM – x positive (x+): 0 = disabled, 1 = enabled

TDOM – y negative (y-): 0 = disabled, 1 = enabled

TUPM – y positive (y+): 0 = disabled, 1 = enabled

TFDM – z negative (z-): 0 = disabled, 1 = enabled

TFUM – z positive (z+): 0 = disabled, 1 = enabled

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER:
		KX224-1053
		Rev. 1.0
		26-Sep-16

INC4

This register controls routing of an interrupt reporting to physical interrupt pin INT1. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
FFI1	BFI1	WMI1	DRDYI1	Reserved	TDTI1	WUFI1	TPI1	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x1Fh								

- FFI1** – Free fall interrupt reported on physical interrupt INT1
- BFI1** – Buffer full interrupt reported on physical interrupt pin INT1
- WMI1** – Watermark interrupt reported on physical interrupt pin INT1
- DRDYI1** – Data ready interrupt reported on physical interrupt pin INT1
- TDTI1** – Tap/Double Tap interrupt reported on physical interrupt pin INT1
- WUFI1** – Wake-Up (motion detect) interrupt reported on physical interrupt pin INT1
- TPI1** – Tilt position interrupt reported on physical interrupt pin INT1

INC5

This register controls the settings for the physical interrupt pin INT2. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PWSEL21	PWSEL20	IEN2	IEA2	IEL2	Reserved	ACLR2	ACLR1	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00010000
I ² C Address: 0x20h								

- PWSEL2<1:0>** – Pulse interrupt 2 width configuration
 - 00 = 50us (10us if OSA > 1600Hz)
 - 01 = 1 * OSA period
 - 10 = 2 * OSA periods
 - 11 = 4 * OSA periods

When PWSEL2 > 0, Interrupt source auto-clearing (ACLR2=1) is strongly recommended to keep consistency between the internal status and the physical interrupt.

- IEN2** enables/disables the physical interrupt pin
 - IEN2 = 0 – physical interrupt pin is disabled
 - IEN2 = 1 – physical interrupt pin is enabled



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

IEA2 sets the polarity of the physical interrupt pin
 IEA2 = 0 – polarity of the physical interrupt pin is active low
 IEA2 = 1 – polarity of the physical interrupt pin is active high

IEL2 sets the response of the physical interrupt pin
 IEL2 = 0 – the physical interrupt pin latches until it is cleared by reading INT_REL
 IEL2 = 1 – the physical interrupt pin will transmit one pulse configurable by PWSEL2

ACLR2 – Interrupt source automatic clear at pulse interrupt 2 trailing edge
 ACLR2 = 0 – disable
 ACLR2 = 1 – enable


ACLR1 – Interrupt source automatic clear at pulse interrupt 1 trailing edge
 ACLR1 = 0 – disable
 ACLR1 = 1 – enable

INC6

This register controls routing of interrupt reporting to physical interrupt pin INT2. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
FFI2	BFI2	WMI2	DRDYI2	Reserved	TDTI2	WUFI2	TPI2	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x21h								

- FFI2** – Free fall interrupt reported on physical interrupt INT2
- BFI2** – Buffer full interrupt reported on physical interrupt pin INT2
- WMI2** – Watermark interrupt reported on physical interrupt pin INT2
- DRDYI2** – Data ready interrupt reported on physical interrupt pin INT2
- TDTI2** - Tap/Double Tap interrupt reported on physical interrupt pin INT2
- WUFI2** – Wake-Up (motion detect) interrupt reported on physical interrupt pin INT2
- TPI2** – Tilt position interrupt reported on physical interrupt pin INT2

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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TILT_TIMER

This register is the initial count register for the tilt position state timer (0 to 255 counts). Every count is calculated as 1/ODR delay period, where the ODR is user-defined per Table 18. A new state must be valid as many measurement periods before the change is accepted. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TSC7	TSC6	TSC5	TSC4	TSC3	TSC2	TSC1	TSC0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x22h								

WUFC

This register is the initial count register for the motion detection timer (0 to 255 counts). Every count is calculated as 1/ODR delay period, where the ODR is user-defined per Table 20. A new state must be valid as many measurement periods before the change is accepted. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
WUFC7	WUFC6	WUFC5	WUFC4	WUFC3	WUFC2	WUFC1	WUFC0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x23h								

TDTRC

This register is responsible for enabling/disabling reporting of Tap/Double Tap. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	DTRE	STRE	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000011
I ² C Address: 0x24h								

DTRE enables/disables the double tap interrupt

DTRE = 0 – do not update/trigger interrupts on double tap events

DTRE = 1 –update interrupts on double tap events

STRE enables/disables single tap interrupt

STRE = 0 – do not update/trigger interrupts on single tap events

STRE = 1 –update interrupts on single tap events

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

TDTC

This register contains counter information for the detection of a double tap event. When the Directional Tap™ ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional Tap™ ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional Tap™ ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional Tap™ ODR is user-defined per Table 19. The TDTC counts starts at the beginning of the first tap and it represents the minimum time separation between the first tap and the second tap in a double tap event. More specifically, the second tap event must end outside of the TDTC. The Kionix recommended default value is 0.3 seconds (0x78h). Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TDTC7	TDTC6	TDTC5	TDTC4	TDTC3	TDTC2	TDTC1	TDTC0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01111000
I ² C Address: 0x25h								

TTH

This register represents the 8-bit jerk high threshold to determine if a tap is detected. Though this is an 8-bit register, the register value is internally multiplied by two in order to set the high threshold. This multiplication results in a range of 0d to 510d with a resolution of two counts. The Performance Index (PI) is the jerk signal that is expected to be less than this threshold, but greater than the TTL threshold during single and double tap events. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”. The Kionix recommended default value is 203 (0xCBh) and the Performance Index is calculated as:

$$X' = X \text{ (current)} - X \text{ (previous)}$$


$$Y' = Y \text{ (current)} - Y \text{ (previous)}$$

$$Z' = Z \text{ (current)} - Z \text{ (previous)}$$

$$PI = |X'| + |Y'| + |Z'|$$

Equation 1: Performance Index

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TTH7	TTH6	TTH5	TTH4	TTH3	TTH2	TTH1	TTH0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	11001011
I ² C Address: 0x26h								

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

TTL

This register represents the 8-bit (0d– 255d) jerk low threshold to determine if a tap is detected. The Performance Index (PI) is the jerk signal that is expected to be greater than this threshold and less than the TTH threshold during single and double tap events. The Kionix recommended default value is 26 (0x1Ah). Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TTL7	TTL6	TTL5	TTL4	TTL3	TTL2	TTL1	TTL0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00011010
I ² C Address: 0x27h								

FTD


This register contains counter information for the detection of any tap event. When the Directional Tap™ ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional Tap™ ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional Tap™ ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional Tap™ ODR is user-defined per Table 19. In order to ensure that only tap events are detected, these time limits are used. A tap event must be above the performance index threshold for at least the low limit (FTDL0 – FTDL2) and no more than the high limit (FTDH0 – FTDH4). The Kionix recommended default value for the high limit is 0.05 seconds and for the low limit is 0.005 seconds (0xA2h). Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
FTDH4	FTDH3	FTDH2	FTDH1	FTDH0	FTDL2	FTDL1	FTDL0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	10100010
I ² C Address: 0x28h								

STD

This register contains counter information for the detection of a double tap event. When the Directional Tap™ ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional Tap™ ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional Tap™ ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional Tap™ ODR is user-defined per Table 19. In order to ensure that only tap events are detected, this time limit is used. This register sets the total amount of time that the two taps in a double tap event can be above the PI threshold (TTL). The Kionix recommended default value for STD is 0.09 seconds (0x24h). Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
STD7	STD6	STD5	STD4	STD3	STD2	STD1	STD0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00100100
I ² C Address: 0x29h								

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

TLT


This register contains counter information for the detection of a tap event. When the Directional Tap™ ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional Tap™ ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional Tap™ ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional Tap™ ODR is user-defined per Table 19. In order to ensure that only tap events are detected, this time limit is used. This register sets the total amount of time that the tap algorithm will count samples that are above the PI threshold (TTL) during a potential tap event. It is used during both single and double tap events. However, reporting of single taps on the physical interrupt pin INT1 or INT2 will occur at the end of the TWS. The Kionix recommended default value for TLT is 0.1 seconds (0x28h). Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TLT7	TLT6	TLT5	TLT4	TLT3	TLT2	TLT1	TLT0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00101000
I ² C Address: 0x2Ah								

TWS

This register contains counter information for the detection of single and double taps. When the Directional Tap™ ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional Tap™ ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional Tap™ ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional Tap™ ODR is user-defined per Table 19. It defines the time window for the entire tap event, single or double, to occur. Reporting of single taps on the physical interrupt pin INT1 or INT2 will occur at the end of this tap window. The Kionix recommended default value for TWS is 0.4 seconds (0xA0h). Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TWS7	TWS6	TWS5	TWS4	TWS3	TWS2	TWS1	TWS0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	10100000
I ² C Address: 0x2Bh								

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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FFTH

Free Fall Threshold: This register contains the threshold of the Free fall detection. This value is compared to the top 8 bits of the accelerometer 8g output. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
FFTH7	FFTH6	FFTH5	FFTH4	FFTH3	FFTH2	FFTH1	FFTH0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x2Ch								

FFC

Free Fall Counter: This register contains the counter setting of the Free fall detection. Every count is calculated as 1/ODR delay period. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
FFC7	FFC6	FFC5	FFC4	FFC3	FFC2	FFC1	FFC0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x2Dh								

FFCNTL

Free Fall Control: This register contains the counter setting of the Free fall detection. Every count is calculated as 1/ODR delay period. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
FFIE	ULMODE	0	0	DCRM	OFFI2	OFFI1	OFFI0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x2Eh								

FFIE – Free fall engine enable

FFIE = 0 – disable

FFIE = 1 – enable

ULMODE – Free fall interrupt latch/un-latch control


ULMODE = 0 – latched

ULMODE = 1 – unlatched

DCRM – Debounce methodology control

DCRM = 0 – count up/down

DCRM = 1 – count up/reset

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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OFFI<2:0>: – Output Data Rate at which the Free fall engine performs its function. The default Free fall ODR is 12.5Hz.

OFFI	Output Data Rate (Hz)
000	12.5
001	25
010	50
011	100
100	200
101	400
110	800
111	1600

ATH

This register sets the threshold for wake-up (motion detect) interrupt is set. The KX224 will ship from the factory with this value set to correspond to a change in acceleration of 0.5g. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ATH7	ATH6	ATH5	ATH4	ATH3	ATH2	ATH1	ATH0	00000010
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
I ² C Address: 0x30h								

TILT_ANGLE_LL

This register sets the low level threshold for tilt angle detection. The KX224 ships from the factory with tilt angle set to a low threshold of 22° from horizontal. A different default tilt angle can be requested from the factory. Note that the minimum suggested tilt angle is 10°. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0	00001100
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
I ² C Address: 0x32h								

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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TILT_ANGLE_HL

This register sets the high level threshold for tilt angle detection. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
HL7	HL6	HL5	HL4	HL3	HL2	HL1	HL0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00101010
I ² C Address: 0x33h								

HYST_SET

This register sets the Hysteresis that is placed in between the Screen Rotation states. The KX224 ships from the factory with HYST_SET set to ±15° of hysteresis. A different default hysteresis can be requested from the factory. Note that when writing a new value to this register the current values of RES0 and RES1 must be preserved. These values are set at the factory and must not change. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RES1	RES0	HYST5	HYST4	HYST3	HYST2	HYST1	HYST0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00010100
I ² C Address: 0x34h								


LP_CNTL

The Averaging Filter Control setting can be used in the optimization of current and noise performance of the accelerometer and can be tested using [Kionix FlexSet™ Performance Optimization Tool](#). More specifically, this setting determines the number of internal acceleration samples to be averaged in Low Current mode. Also, it determines the number of internal acceleration samples to be averaged for digital engines operation (Directional Tap™, Tilt, Wake-Up, Freefall) both in *High Resolution* and *Low Current* modes. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	AVC2	AVC1	AVC0	Reserved	Reserved	Reserved	Reserved	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01001011
I ² C Address: 0x35h								

AVC<2:0> – Averaging Filter Control. The default setting is 16 samples and was found to work for most case. 000 = No Averaging 000 = No Averaging

- 001 = 2 Samples Averaged
- 010 = 4 Samples Averaged
- 011 = 8 Samples Averaged
- 100 = 16 Samples Averaged (default)

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

101 = 32 Samples Averaged
110 = 64 Samples Averaged
111 = 128 Samples Averaged

BUF_CNTL1


Read/write control register that controls the buffer sample threshold. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
SMP_TH7	SMP_TH6	SMP_TH5	SMP_TH4	SMP_TH3	SMP_TH2	SMP_TH1	SMP_TH0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x3Ah								

SMP_TH[9:0] Sample Threshold; determines the number of samples that will trigger a watermark interrupt or will be saved prior to a trigger event. When BUF_RES=1, the maximum number of samples is 340; when BUF_RES=0, the maximum number of samples is 681.

Buffer Model	Sample Function
Bypass	None
FIFO	Specifies how many buffer samples are needed to trigger a watermark interrupt.
Stream	Specifies how many buffer samples are needed to trigger a watermark interrupt.
Trigger	Specifies how many buffer samples before the trigger event are retained in the buffer.
FILO	Specifies how many buffer samples are needed to trigger a watermark interrupt.

Table 22: Sample Threshold Operation by Buffer Mode

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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BUF_CNTL2

Read/write control register that controls sample buffer operation. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BUFE	BRES	BFIE	0	SMP_TH9	SMP_TH8	BUF_M1	BUF_M0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x3Bh								

BUFE controls activation of the sample buffer.

BUFE = 0 – sample buffer inactive

BUFE = 1 – sample buffer active

BRES determines the resolution of the acceleration data samples collected by the sample buffer.

BUF_RES = 0 – 8-bit samples are accumulated in the buffer

BUF_RES = 1 – 16-bit samples are accumulated in the buffer

BFIE buffer full interrupt enable bit

BFIE = 0 – buffer full interrupt disabled

BFIE = 1 – buffer full interrupt updated in INS2

BUF_M1, BUF_M0 selects the operating mode of the sample buffer per Table 23.

BUF_M1	BUF_M0	Mode	Description
0	0	FIFO	The buffer collects 681 sets of 8-bit low resolution values or 340 sets of 16-bit high resolution values and then stops collecting data, collecting new data only when the buffer is not full.
0	1	Stream	The buffer holds the last 681 sets of 8-bit low resolution values or 340 sets of 16-bit high resolution values. Once the buffer is full, the oldest data is discarded to make room for newer data.
1	0	Trigger	When a trigger event occurs, the buffer holds the last data set of SMP_TH[9:0] samples before the trigger event and then continues to collect data until full. New data is collected only when the buffer is not full.
1	1	FILO	The buffer holds the last 681 sets of 8-bit low resolution values or 340 sets of 16-bit high resolution values. Once the buffer is full, the oldest data is discarded to make room for newer data. Reading from the buffer in this mode will return the most recent data first.

Table 23: Selected Buffer Mode

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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BUF_STATUS_1

This register reports the status of the sample buffer.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SMP_LEV7	SMP_LEV6	SMP_LEV5	SMP_LEV4	SMP_LEV3	SMP_LEV2	SMP_LEV1	SMP_LEV0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x3Ch							

SMP_LEV[10:0] Sample Level; reports the number of *data bytes* that have been stored in the sample buffer. When *BUF_RES=1*, this count will increase by 6 for each 3-axis sample in the buffer; when *BUF_RES=0*, the count will increase by 3 for each 3-axis sample. If this register reads 0, no data has been stored in the buffer.

BUF_STATUS_2

This register reports the status of the sample buffer trigger function.


R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BUF_TRIG	0	0	0	0	SMP_LEV10	SMP_LEV9	SMP_LEV8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x3Dh							

BUF_TRIG reports the status of the buffer's trigger function if this mode has been selected. When using trigger mode, a buffer read should only be performed after a trigger event. This bit is also gets cleared after writing to *BUF_CLEAR* register. This will prevent Buffer Full interrupt from firing while *TRIG* pin remains deasserted.

BUF_CLEAR

When any data is written to this register, the entire sample buffer is cleared. This causes the sample level bits *SMP_LEV[10:0]* to be cleared in *BUF_STATUS_1* and *BUF_STATUS_2* registers. In addition, if the sample buffer is set to Trigger mode, the *BUF_TRIG* bit in *BUF_STATUS_2* is cleared too. Finally, the *BFI* and *WMI* bits in *INS2* will be cleared and physical interrupt latched pin will be changed to its inactive state.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x3Eh							

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

BUF_READ

Buffer output register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I ² C Address: 0x3Fh							


Note: new data is not being written to the buffer during the buffer read operation. Thus, care must be taken when reading from the buffer. If data loss is not desired, the buffer read operation should be completed within ODR clock cycle.

SELF_TEST

When 0xCA is written to this register, the MEMS self-test function is enabled. Electrostatic-actuation of the accelerometer, results in a DC shift of the X, Y and Z axis outputs. Writing 0x00 to this register will return the accelerometer to normal operation.

****Note, this is a write-only register. Read back value from this register will always be 0x00.**

W	W	W	W	W	W	W	W	W
1	1	0	0	1	0	1	0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
I ² C Address: 0x60h								

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

Embedded Applications

Orientation Detection Feature

The orientation detection feature of the KX224 will report changes in face up, face down, ± vertical and ± horizontal orientation. This intelligent embedded algorithm considers very important factors that provide accurate orientation detection from low cost tri-axis accelerometers. Factors such as: hysteresis, device orientation angle and delay time are described below as these techniques are utilized inside the KX224.

Hysteresis

A 45° tilt angle threshold seems like a good choice because it is halfway between 0° and 90°. However, a problem arises when the user holds the device near 45°. Slight vibrations, noise and inherent sensor error will cause the acceleration to go above and below the threshold rapidly and randomly, so the screen will quickly flip back and forth between the 0° and the 90° orientations. This problem is avoided in the KX224 by choosing a 30° threshold angle. With a 30° threshold, the screen will not rotate from 0° to 90° until the device is tilted to 60° (30° from 90°). To rotate back to 0°, the user must tilt back to 30°, thus avoiding the screen flipping problem. This example essentially applies ± 15° of hysteresis in between the four screen rotation states. Table 24 shows the acceleration limits implemented for $\phi_T = 30^\circ$.

Orientation	X Acceleration (g)	Y Acceleration (g)
0°/360°	$-0.5 < a_x < 0.5$	$a_y > 0.866$
90°	$a_x > 0.866$	$-0.5 < a_y < 0.5$
180°	$-0.5 < a_x < 0.5$	$a_y < -0.866$
270°	$a_x < -0.866$	$-0.5 < a_y < 0.5$

Table 24: Acceleration at the four orientations with ± 15° of hysteresis

The KX224 allows the user to change the amount of hysteresis in between the four screen rotation states. By simply writing to the HYST_SET register, the user can adjust the amount of hysteresis up to ± 45°. The plot in Figure 8 shows the typical amount of hysteresis applied for a given digital count value of HYST_SET.



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

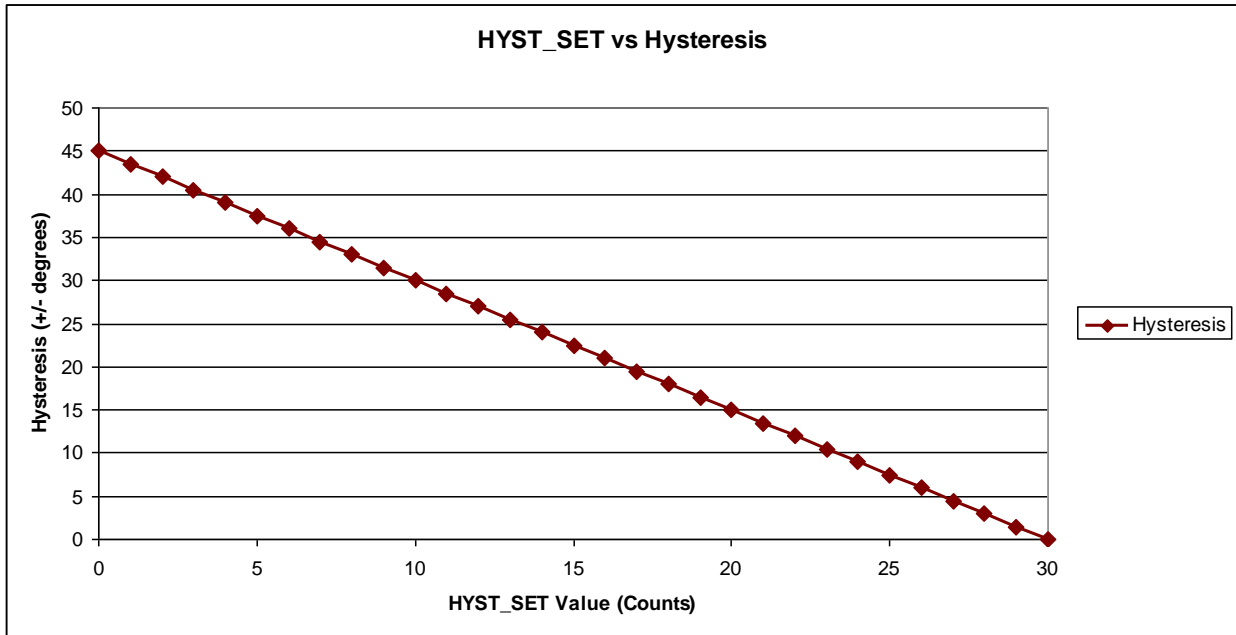


Figure 8: HYST_SET vs Hysteresis

Device Orientation Angle (aka Tilt Angle)

To ensure that horizontal and vertical device orientation changes are detected, even when it isn't in the ideal vertical orientation – where the angle θ in Figure 9 is 90° , the KX224 considers device orientation angle in its algorithm.

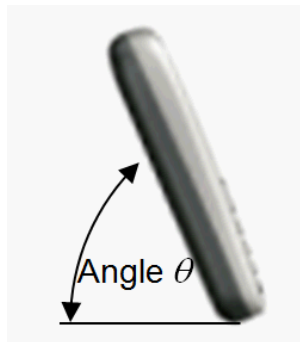



Figure 9: Device Orientation Angle

As the angle in Figure 9 is decreased, the maximum gravitational acceleration on the X-axis or Y-axis will also decrease. Therefore, when the angle becomes small enough, the user will not be able to make the screen orientation change. When the device orientation angle approaches 0° (device is flat on a desk

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

or table), $a_x = a_y = 0g$, $a_z = +1g$, and there is no way to determine which way the screen should be oriented, the internal algorithm determines that the device is in either the face-up or face-down orientation, depending on the sign of the z-axis. The KX224 will only change the screen orientation when the orientation angle is above the factory-defaulted/user-defined threshold set in the TILT_ANGLE_LL register. Equation 2 can be used to determine what value to write to the TILT_ANGLE_LL register to set the device orientation angle. The value for TILT_ANGLE_HL is preset at the factory but can be adjusted in special cases (e.g. to reduce the effect of transient g-variation such as when device is being moved rather than just being rotated).

$$\text{TILT_ANGLE_LL (counts)} = \sin \theta * (32 \text{ (counts/g)})$$


Equation 2: Tilt Angle Threshold

Tilt Timer

The 8-bit register, TILT_TIMER can be used to qualify changes in orientation. The KX224 does this by incrementing a counter with a size that is specified by the value in TILT_TIMER for each set of acceleration samples to verify that a change to a new orientation state is maintained. A user defined output data rate (ODR) determines the time period for each sample. Equation 3 shows how to calculate the TILT_TIMER register value for a desired delay time.

$$\text{TILT_TIMER (counts)} = \text{Delay Time (sec)} \times \text{ODR (Hz)}$$

Equation 3: Tilt Position Delay Time

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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Motion Interrupt Feature Description

The Motion interrupt feature of the KX224 reports qualified changes in the high-pass filtered acceleration based on the Wake Up (ATH) threshold. If the high-pass filtered acceleration on any axis is greater than the user-defined wake up threshold (ATH), the device has transitioned from an inactive state to an active state. Equation 4 shows how to calculate the ATH register value for a desired wake up threshold.

$$\text{ATH (counts)} = \text{Wake Up Threshold (g)} \times 4 \text{ (counts/g)}$$

Equation 4: Wake Up Threshold

An 8-bit raw unsigned value represents a counter that permits the user to qualify each active/inactive state change. Note that each WUFC Timer count qualifies 1 (one) user-defined ODR period (OWUF). Equation 5 shows how to calculate the WUFC register value for a desired wake up delay time.

$$\text{WUFC (counts)} = \text{Wake Up Delay Time (sec)} \times \text{OWUF (Hz)}$$

Equation 5: Wake Up Delay Time

The latched motion interrupt response algorithm works as following: while the part is in inactive state, the algorithm evaluates differential measurement between each new acceleration data point with the preceding one and evaluates it against the ATH threshold. When the differential measurement is greater than ATH threshold, the wakeup counter starts the count. Differential measurements are now calculated based on the difference between the current acceleration and the acceleration when the counter started. The part will report that motion has occurred at the end of the count assuming each differential measurement has remained above the threshold. If at any moment during the count the differential measurement falls below the threshold, the counter will stop the count and the part will remain in inactive state.

To illustrate how the algorithm works, consider the Figure 10 below that shows the latched response of the motion detection algorithm with WUF Timer (WUFC) set to 10 counts. Note how the difference between the acceleration sample marked in red and the one marked in green resulted in a differential measurements represented with orange bar being above the WUF threshold. At this point, the counter begins to count number of counts stored in WUFC register and the wakeup algorithm will evaluate the difference between each new acceleration measurement and the measurement marked in green that will remain a reference measurement for the duration of the counter count. At the end of the count, assuming all differential measurements were larger than WUF threshold, as is the case in the example showed in Figure 10, a motion event will be reported.



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

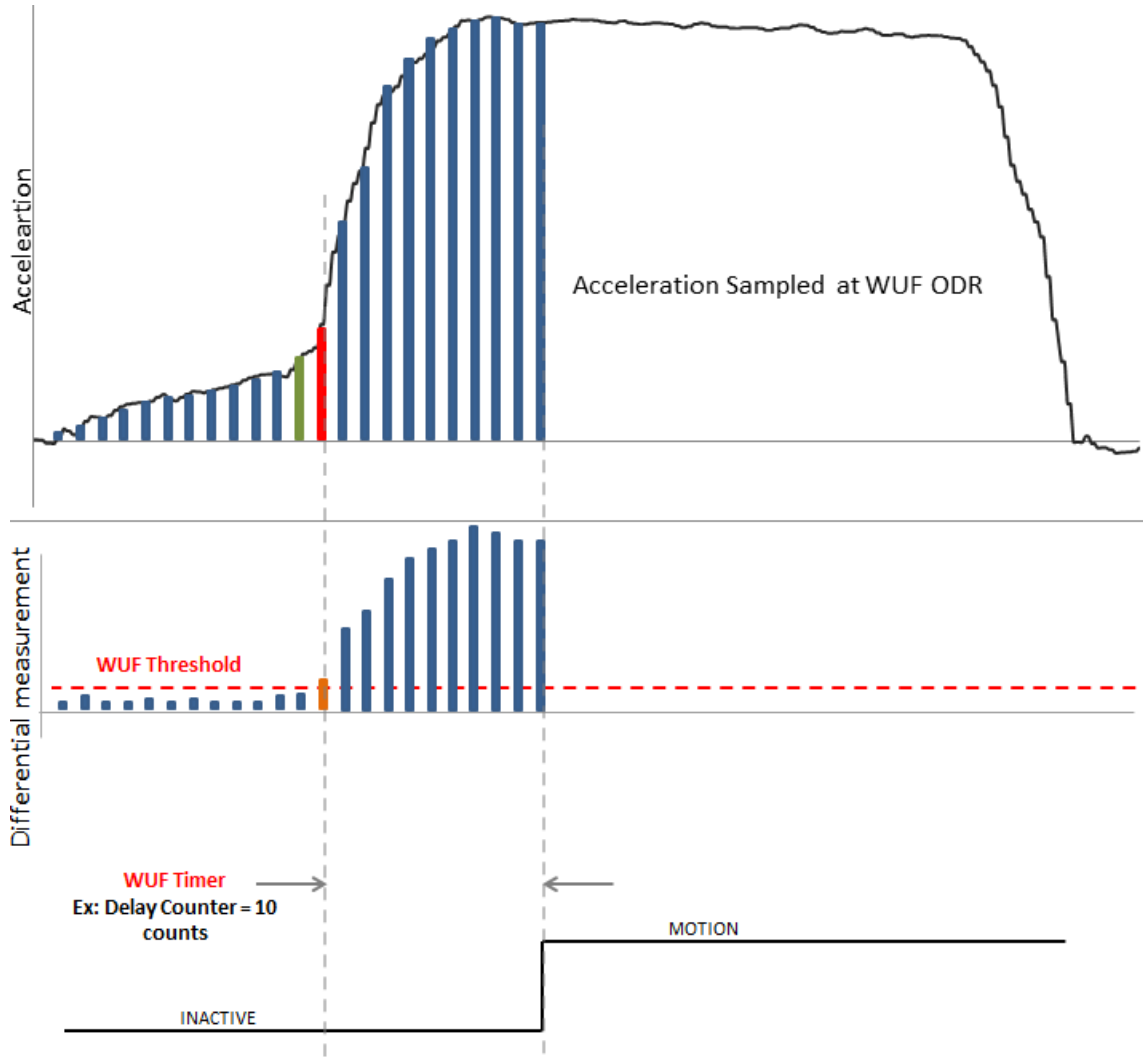



Figure 10: Latched Motion Interrupt Response

	<p align="center">± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications</p>	<p>PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16</p>
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Directional Tap Detection Feature Description

The Directional Tap Detection feature of the KX224 recognizes single and double tap inputs and reports the acceleration axis and direction that each tap occurred. Eight performance parameters, as well as a user-selectable ODR are used to configure the KX224 for a desired tap detection response.

Performance Index

The Directional Tap™ detection algorithm uses low and high thresholds to help determine when a tap event has occurred. A tap event is detected when the previously described jerk summation exceeds the low threshold (TTL) for more than the tap detection low limit, but less than the tap detection high limit as contained in FTD. Samples that exceed the high limit (TTH) will be ignored. Figure 11 shows an example of a single tap event meeting the performance index criteria.

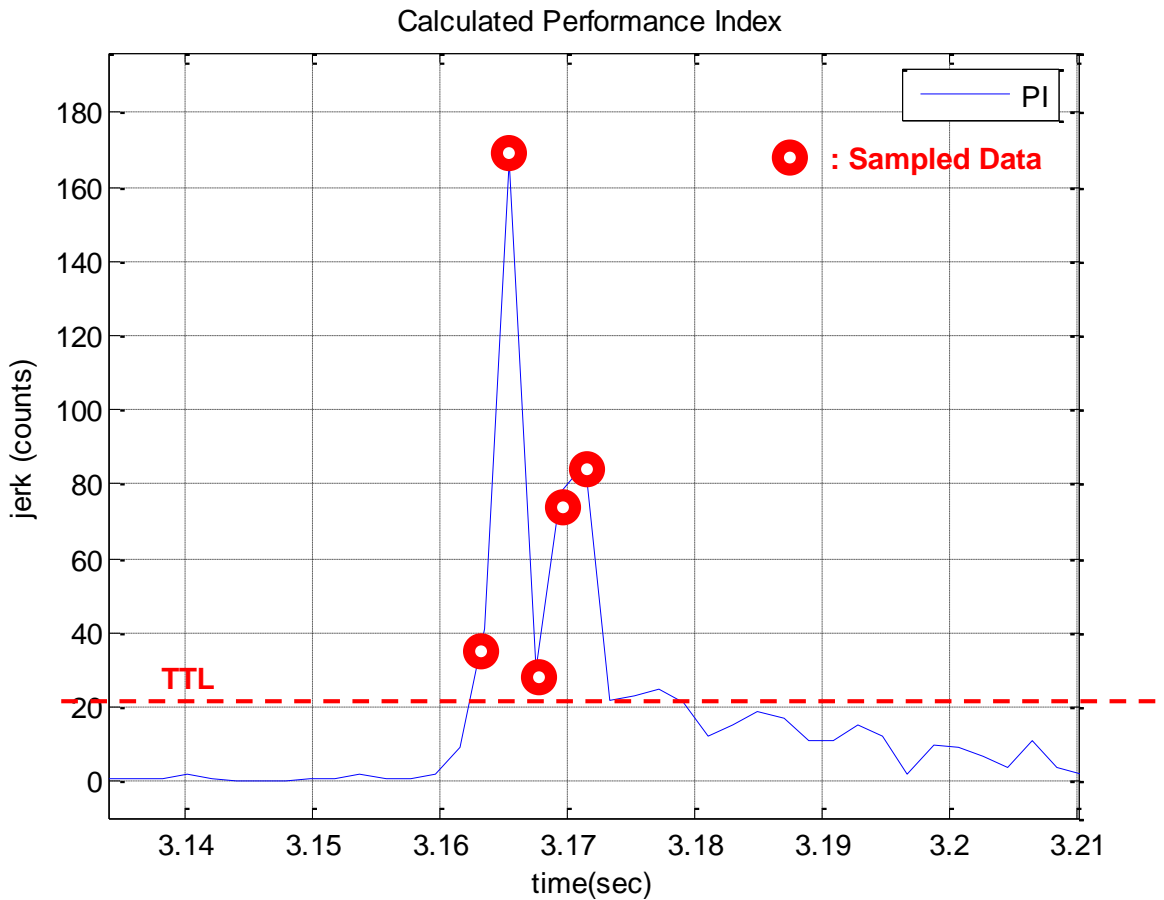


Figure 11: Jerk Summation vs Threshold



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

Single Tap Detection

The latency timer (TLT) sets the time period that a tap event will only be characterized as a single tap. A second tap has to occur outside of the latency timer. If a second tap occurs inside the latency time, it will be ignored as it occurred too quickly. The single tap will be reported at the end of the TWS. Figure 12 shows a single tap event meeting the PI, latency and window requirements.

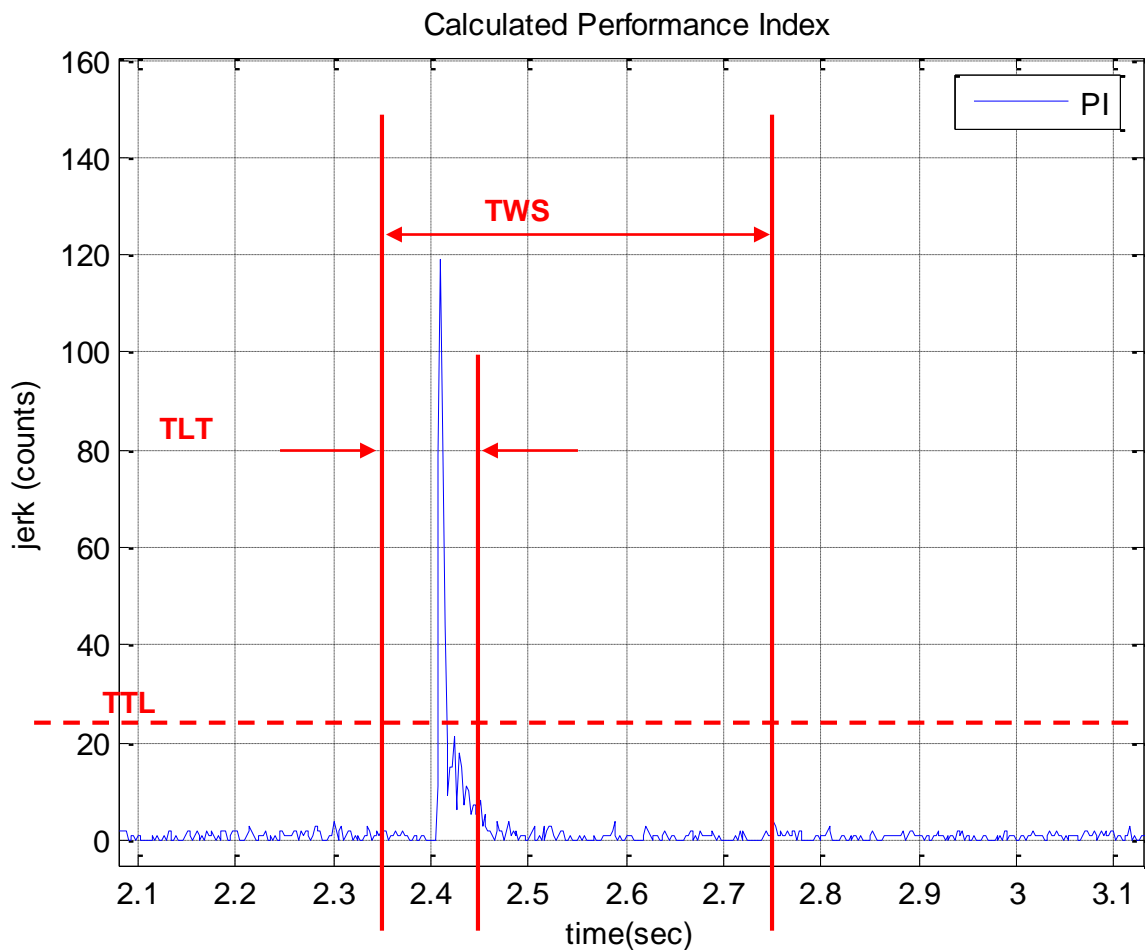


Figure 12: Single Directional TapTM Timing



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

Double Tap Detection

An event can be characterized as a double tap if the second tap crosses the performance index (TTL) inside the TWS period and ends outside the TDTC. This means that the TDTC determines the minimum time separation that must exist between the two taps of a double tap event. Similar to the single tap, the first tap event must exceed the performance index for the time limit contained in FTD. Also, the duration when the first and second events combined exceed the performance index should not exceed STD. The double tap will be reported at the end of the second TLT. Figure 13 shows a double tap event meeting the PI, latency and window requirements.

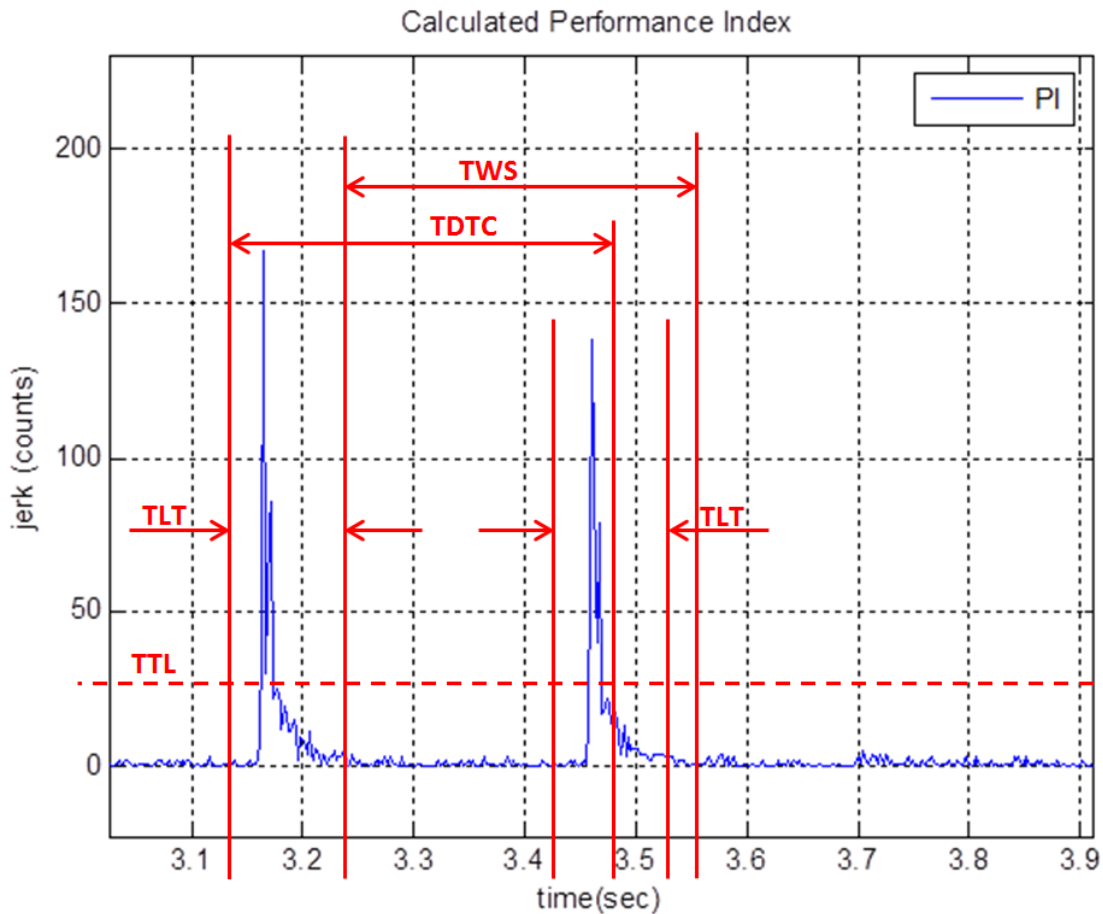



Figure 13: Double Directional TapTM Timing

	<p align="center">± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications</p>	<p>PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16</p>
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Free fall Detect

The KX224 features a Free fall interrupt that sends a flag through INT1 or INT2 when the accelerometer senses a Free fall event. A Free fall event is evident when all three accelerometer axes simultaneously fall below a certain acceleration threshold for a set amount of time. The KX224 gives the user the option to define the acceleration threshold value through the FFTH 8-bit register where 256 counts cover the g range of the accelerometer. This value is compared to the top 8 bits of the accelerometer 8g output.

Through the Free Fall Counter (FFC), the user can set the amount of time all three accelerometer axes must simultaneously remain below the FFTH acceleration threshold before the Free fall interrupt flag is sent through INT1 or INT2. This delay/debounce time is defined by the available 0 to 255 counts, which represent accelerometer samples taken at the rate defined by OFFI<2:0>. Every count is calculated as 1/ODR delay period.

When the Free fall interrupt is enabled the part must not be in a physical state that would trigger the Free fall interrupt or the delay will not be correct for the present Free fall.



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

Typical Freefall Interrupt Example (nonLatching)

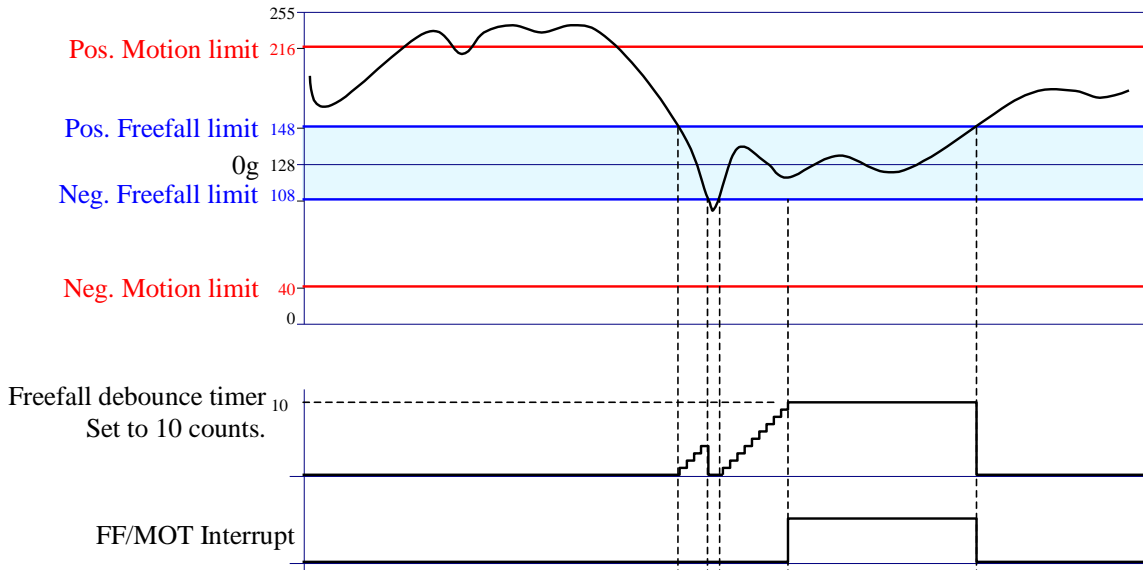


Figure 14: Typical Free fall Interrupt Example (FFC ULMODE = 1)

Typical Freefall Interrupt Example (Latching)

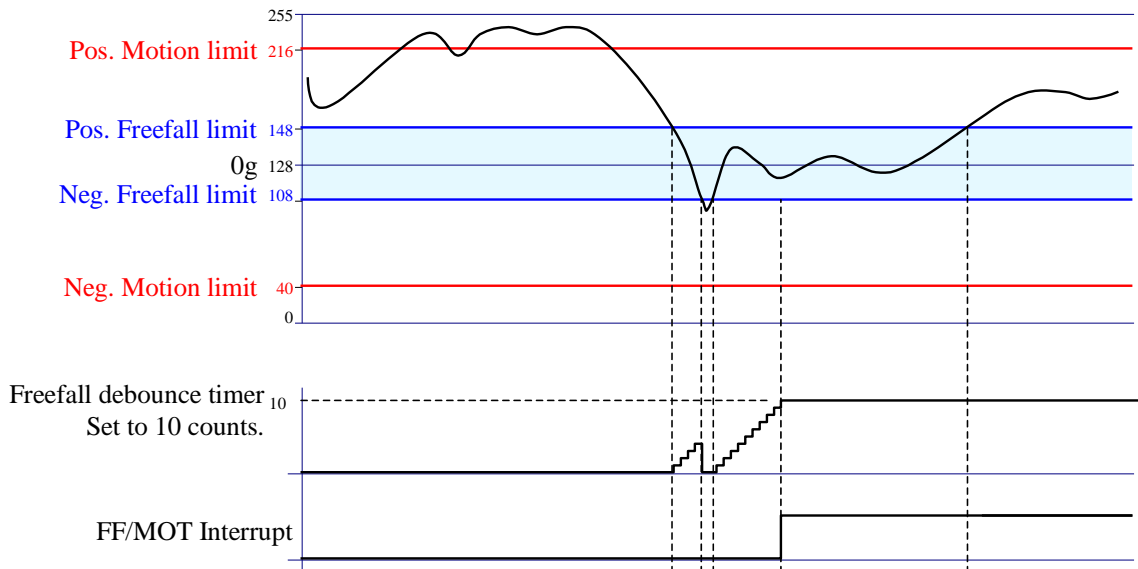



Figure 15: Typical Free fall Interrupt Example (FFC ULMODE = 0)

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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Sample Buffer Feature Description

The sample buffer feature of the KX224 accumulates and outputs acceleration data based on how it is configured. There are 4 buffer modes available, and samples can be accumulated at either low (8-bit) or high (16-bit) resolution. Acceleration data is collected at the ODR specified by OSA[3:0] in the ODCNTL register. Each buffer mode accumulates data, reports data, and interacts with status indicators in a slightly different way.

FIFO Mode

Data Accumulation

Sample collection stops when the buffer is full.

Data Reporting

Data is reported with the oldest byte of the oldest sample first (X_L or X based on resolution).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 6).

BUF_RES=0:

$$\text{SMPX} = \text{SMP_LEV}[10:0] / 3 - \text{SMP_TH}[9:0]$$

BUF_RES=1:

$$\text{SMPX} = \text{SMP_LEV}[10:0] / 6 - \text{SMP_TH}[9:0]$$

Equation 6: Samples Above Sample Threshold

Stream Mode

Data Accumulation


Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 6).

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

Trigger Mode

Data Accumulation

When a physical interrupt is caused by one of the digital engines or when a logic high signal occurs on the TRIG pin, the trigger event is asserted and SMP_TH[9:0] samples prior to the event are retained. Sample collection continues until the buffer is full.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

When a physical interrupt occurs and there are at least SMP_TH[9:0] samples in the buffer, BUF_TRIG in BUF_STATUS_2 is asserted.

FILO Mode

Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting

Data is reported with the newest byte of the newest sample first (Z_H or Z based on resolution).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 6).

Buffer Operation

The following diagrams illustrate the operation of the buffer conceptually. Actual physical implementation has been abstracted to offer a simplified explanation of how the different buffer modes operate. Figure 16 represents a high-resolution 3-axis sample within the buffer. Figure 17 – Figure 25 represent a 10-sample version of the buffer (for simplicity), with Sample Threshold set to 8.

Regardless of the selected mode, the buffer fills sequentially, one byte at a time. Figure 16 shows one 6-byte data sample. Note the location of the FILO read pointer versus that of the FIFO read pointer.



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

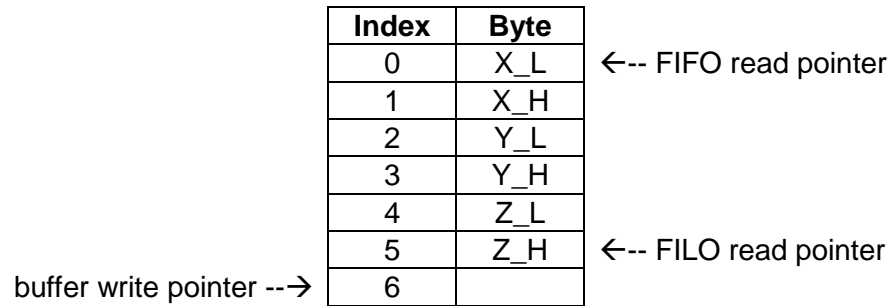


Figure 16: One Buffer Sample

Regardless of the selected mode, the buffer fills sequentially, one sample at a time. Note in Figure 17 the location of the FILO read pointer versus that of the FIFO read pointer. The buffer write pointer shows where the next sample will be written to the buffer.

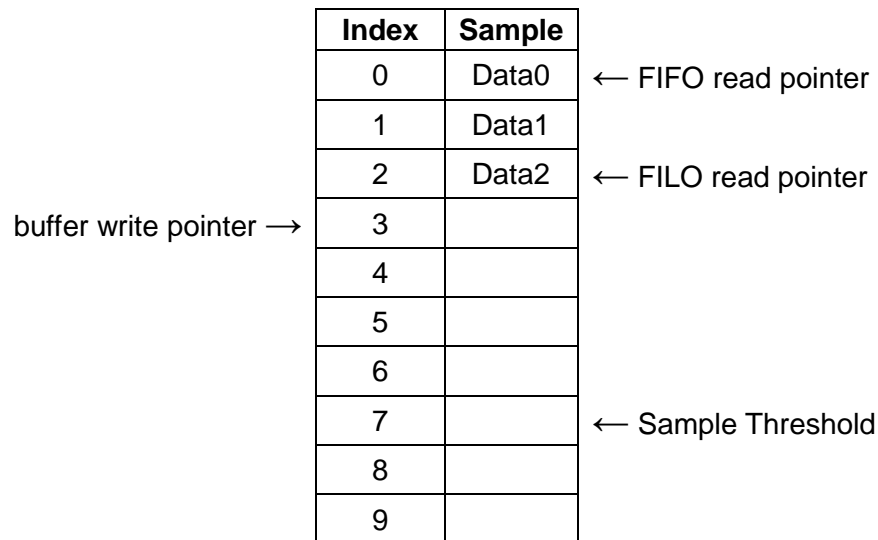


Figure 17: Buffer Filling

The buffer continues to fill sequentially until the Sample Threshold is reached. Note in Figure 18 the location of the FILO read pointer versus that of the FIFO read pointer.

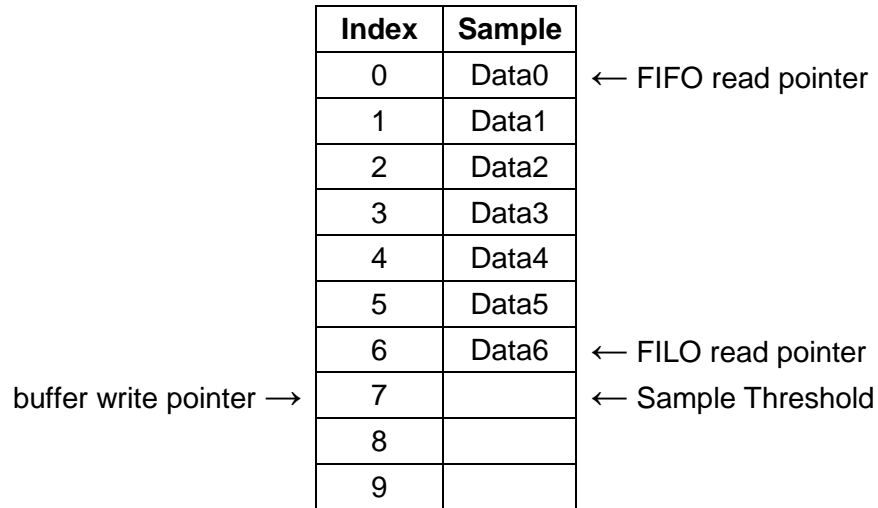


Figure 18: Buffer Approaching Sample Threshold

In FIFO, Stream, and FILO modes, a watermark interrupt is issued when the number of samples in the buffer reaches the Sample Threshold. In trigger mode, this is the point where the oldest data in the buffer is discarded to make room for newer data.

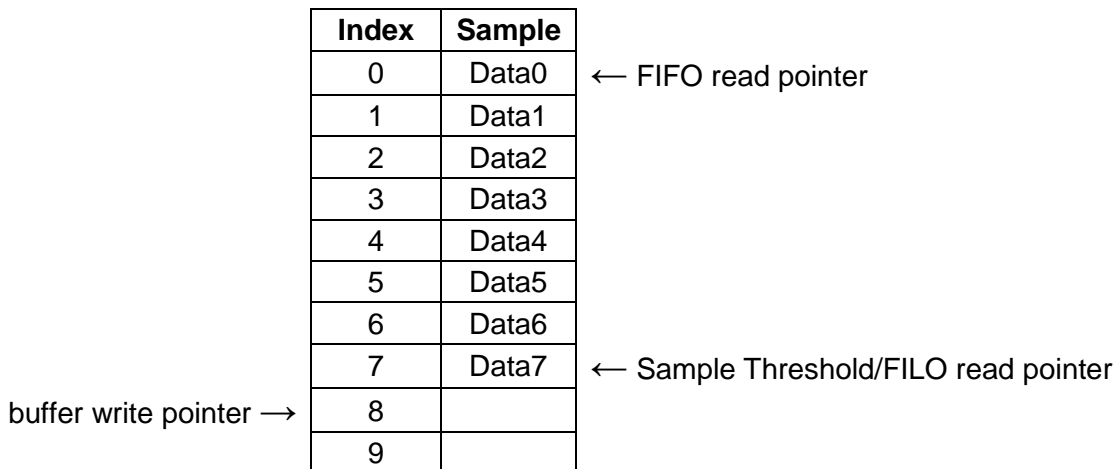


Figure 19: Buffer at Sample Threshold



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

In trigger mode, data is accumulated in the buffer sequentially until the Sample Threshold is reached. Once the Sample Threshold is reached, the oldest samples are discarded when new samples are collected. Note in Figure 20 how Data0 was thrown out to make room for Data8.

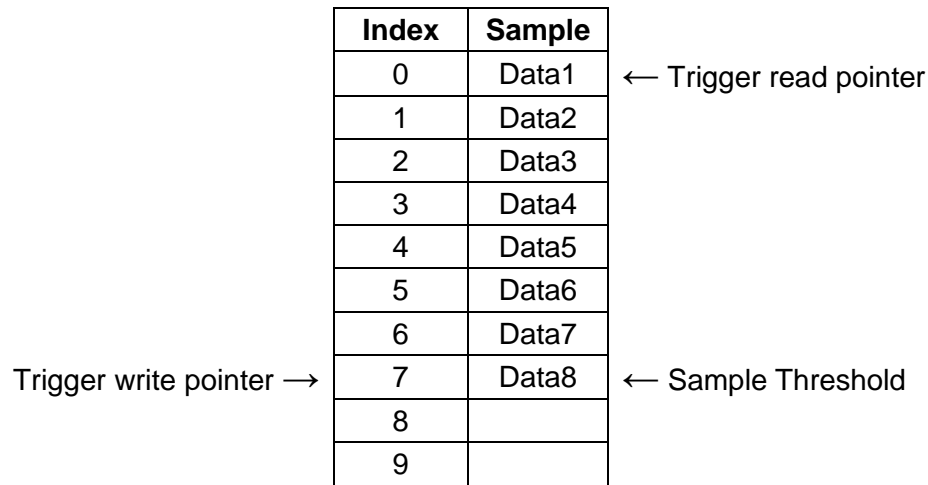


Figure 20: Additional Data Prior to Trigger Event

After a trigger event occurs, the buffer no longer discards the oldest samples, and instead begins accumulating samples sequentially until full. The buffer then stops collecting samples, as seen in Figure 21. This results in the buffer holding SMP_TH[9:0] samples prior to the trigger event, and SMPX samples after the trigger event.

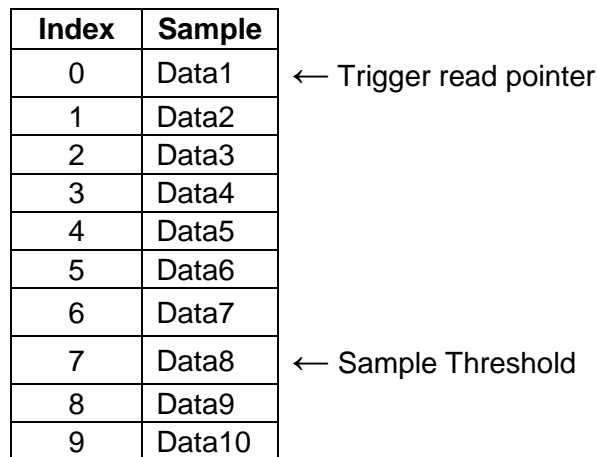



Figure 21: Additional Data after Trigger Event

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

In FIFO, Stream, FILO, and Trigger (after a trigger event has occurred) modes, the buffer continues filling sequentially after the Sample Threshold is reached. Sample accumulation after the buffer is full depends on the selected operation mode. FIFO and Trigger modes stop accumulating samples when the buffer is full, and Stream and FILO modes begin discarding the oldest data when new samples are accumulated.

Index	Sample	
0	Data0	← FIFO read pointer
1	Data1	
2	Data2	
3	Data3	
4	Data4	
5	Data5	
6	Data6	
7	Data7	← Sample Threshold
8	Data8	
9	Data9	← FILO read pointer

Figure 22: Buffer Full

After the buffer has been filled in FILO or Stream mode, the oldest samples are discarded when new samples are collected. Note in Figure 21 how Data0 was thrown out to make room for Data10.

Index	Sample	
0	Data1	← FIFO read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	
6	Data7	
7	Data8	← Sample Threshold
8	Data9	
9	Data10	← FILO read pointer

Figure 23: Buffer Full – Additional Sample Accumulation in Stream or FILO Mode



± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications

PART NUMBER:
KX224-1053
Rev. 1.0
26-Sep-16

In FIFO, Stream, or Trigger mode, reading one sample from the buffer will remove the oldest sample and effectively shift the entire buffer contents up, as seen in Figure 24.

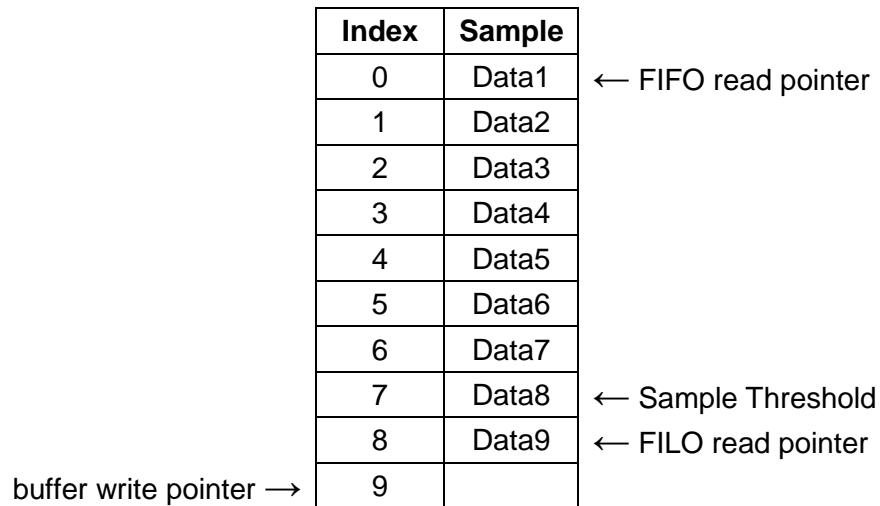


Figure 24: FIFO Read from Full Buffer

In FILO mode, reading one sample from the buffer will remove the newest sample and leave the older samples untouched, as seen in Figure 25.

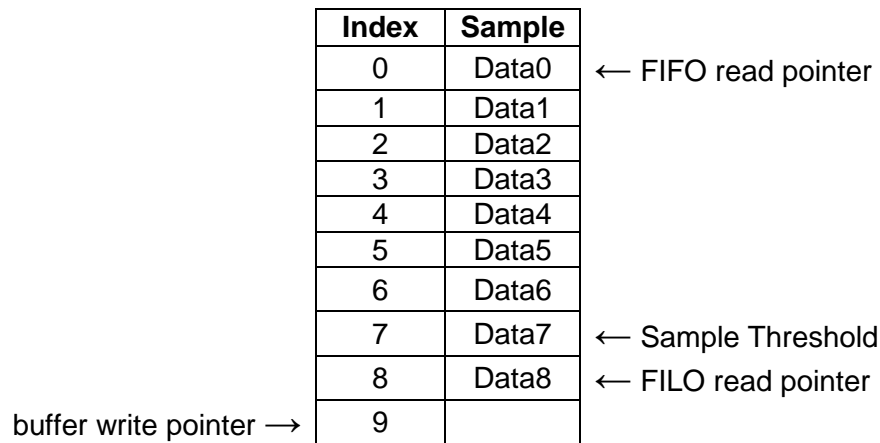




Figure 25: FILO Read from Full Buffer

	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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Revision History

REVISION	DESCRIPTION	DATE
1.0	Initial Release	26-Sep-2016

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	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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CLASS IV		CLASS III	

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	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
---	---	---

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	± 8g / 16g / 32g Tri-axis Digital Accelerometer Specifications	PART NUMBER: KX224-1053 Rev. 1.0 26-Sep-16
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