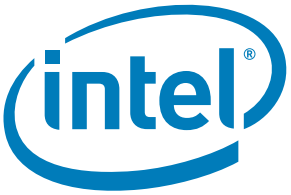
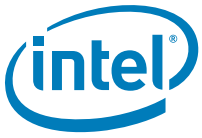


Intel® Xeon® Processor 5600 Series

Datasheet, Volume 1

March 2010

Reference Number: 323369-001



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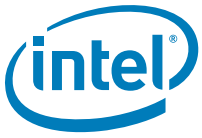

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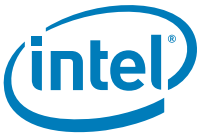

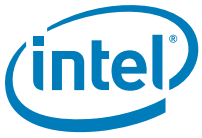

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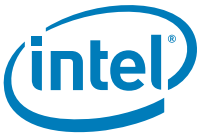

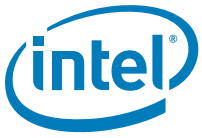

Revision History

Revision Number	Description	Date
-001	• Initial Release	March 2010

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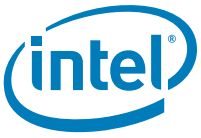
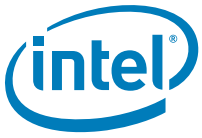




1 Introduction

The Intel® Xeon® processor 5600 series is a server/workstation multi-core processor based on 32 nm process technology. The processors feature two Intel® QuickPath Interconnect point-to-point links capable of up to 6.4 GT/s, up to 12 MB of shared cache, and an Integrated Memory Controller. The processors are optimized for performance with the power efficiencies of a low-power microarchitecture to enable smaller, quieter systems.

This datasheet provides DC and AC electrical specifications, signal integrity, differential signaling specifications, pinout and signal definitions, package mechanical specifications and thermal requirements, and additional features pertinent to implementation and operation of the processor.

The Intel Xeon processor 5600 series features a range of Thermal Design Power (TDP) envelopes from 40W TDP up to 130W TDP, and is segmented into multiple platforms:

- 2-Socket Frequency Optimized Server/Workstation Platforms support a 130 W Thermal Design Power (TDP) SKU and up to 6 core support. These platforms provide optimal overall performance and reliability, in addition to high-end graphics support.
- 2-Socket Advanced Server/Workstation Platforms support a 95 W Thermal Design Power (TDP) SKU. These platforms provide optimal overall performance featuring up to 6 core support.
- 2-Socket Standard Server/Workstation Platforms support 80 W TDP processor SKUs supporting up to 6 cores. These platforms provide optimal performance per watt for rack-optimized platforms.
- Low Power Platforms implement 60 W TDP (up to 6 cores) and 40 W TDP (up to 4 cores) processor SKU's. These processors are intended for dual-processor server blades and embedded servers.
- 1-Socket Workstation Platforms support Intel® Xeon® Processor W3680. These platforms enable a wide range of options for either the performance, power, or cost sensitive customer.
- Platforms supporting Higher Case Temperature Low-Voltage Processors with 60 W TDP (up to 6 cores) and 40 W TDP (up to 4 cores). The higher case temperatures are intended to meet the short-term thermal profile requirements of NEBS Level 3. These 2-socket processors are ideal for thermally-constrained form factors in embedded servers, communications and storage markets. Specifications denoted as LV-60W apply to the Intel® Xeon® Processor L5638. Specifications denoted as LV-40W apply to the Intel® Xeon® Processor L5618.

Note: All references to "chipset" in this document pertain to the Intel® 5520 chipset and the Intel® 5500 chipset.

Intel is committed to delivering processors for both server and workstation platforms that maximize performance while meeting all Intel Quality and Reliability goals. The product's reliability assessment is based on a datasheet compliant system and reference use condition. Intel utilizes a broad set of use condition assumptions (i.e. percentage of time in active vs. inactive operation, non-operating conditions, and the number of power cycles per year) to ensure proper operation over the life of the

product. The reference use condition differs between workstation and server processor SKU's. Implementing processors outside of reference use conditions may affect reliability performance.

1.1 Processor Features

Table 1-1 provides an overview the Intel Xeon processor 5600 series feature set.

Table 1-1. Intel® Xeon® Processor 5600 Series Feature Set Overview

Feature	Intel® Xeon® Processor 5600 Series
Cache Sizes	Instruction Cache: 32 kB Data Cache: 32 kB 256 kB Mid-Level Cache per core 12 MB Last-Level Cache shared among all cores
Data Transfer Rate (GT/s)	Two full-width Intel® QuickPath Interconnect links; Up to 6.40 GT/s in each direction
Memory Support	Integrated Memory Controller supports up to 3 channels of DDR3 or DDR3L memory, with up to 3 DIMMs per channel
DDR3 Memory Speed (MHz)	800, 1066, 1333
Multi-Core Support	Up to 6 cores per processor (package)
Intel® Hyper-Threading Technology	2 threads per core
Dual Processor Support	Up to 2 processor sockets per platform
Package	1366-land FC-LGA

The Intel Xeon processor 5600 series support all the existing Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3) and Streaming SIMD Extensions 4 (SSE4) instructions. Additionally, Intel Xeon processor 5600 series support Advanced Encryption Standard-New Instructions (AES-NI).

The Intel Xeon processor 5600 series support Direct Cache Access (DCA). DCA enables supported I/O adapter to pre-fetch data from memory to the processor cache, thereby avoiding cache misses and improving application response times.

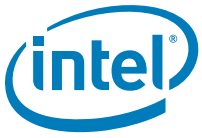
These processors support a maximum physical address size of 40 bits. Also supported is IA-32e paging which adds support for 1 GB (2^{30}) page size in addition to 2 MB and 4 kB page size support for linear to physical address translation.

Finally, these processors support several advanced technologies including Execute Disable Bit, Intel® 64 Technology, Enhanced Intel SpeedStep® Technology, Intel® Virtualization Technology (Intel® VT), Intel® Hyper-Threading Technology, and Intel® Turbo Boost Technology.

1.2 Platform Features

Various new component and platform capabilities are available with the implementation of Intel Xeon processor 5600 series.

New memory subsystem capabilities include Low Voltage DDR3 (DDR3L) DIMM support for power optimization. The Intel Xeon processor 5600 series also add features to provide improved manageability of memory channels. The DDR_THERM2# signal has been added to support high-temperature DIMMs and their 2X refresh requirements.



Intel Xeon processor 5600 series are based on a low-power micro-architecture that supports operation within various C-states. Additionally, six execution cores and power management coordination logic are optimized to manage C-state support at both the execution core and package levels. An Intel Turbo Boost Technology optimization feature is supported on these processors for improved energy efficiency.

Intel® Trusted Execution Technology (Intel® TXT) is also supported and represents a set of enhanced hardware components designed to help protect sensitive information from software-based attacks. Features include capabilities in the microprocessor, chipset, I/O subsystems, and other platform components. When coupled with suitably enabled operating systems and applications, Intel® TXT helps protect the confidentiality and integrity of data in the face of increasingly hostile security environment.

1.3 Terminology

A '#' symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low voltage level. For example, when RESET# is low, a reset has been requested.

A '_N' and '_P' after a signal name refers to a differential pair.

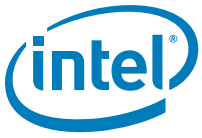
Commonly used terms are explained here for clarification:

- **1366-land FC-LGA package** — The Intel Xeon processor 5600 series is available in a Flip-Chip Land Grid Array (FC-LGA) package, consisting of processor mounted on a land grid array substrate with an integrated heat spreader (IHS).
- **DDR3** — Double Data Rate 3 synchronous dynamic random access memory (SDRAM) is the DDR memory standard, developed as the successor to DDR2 SDRAM.
- **Enhanced Intel SpeedStep® Technology** — Enhanced Intel SpeedStep® Technology allows the operating system to reduce power consumption when performance is not needed.
- **Execute Disable Bit** — Execute Disable allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer over run vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architecture Software Developer's Manuals* for more detailed information.
- **Functional Operation** — Refers to the normal operating conditions in which all processor specifications, including DC, AC, signal quality, mechanical, and thermal, are satisfied.
- **Integrated Memory Controller (IMC)** — This is a memory controller that is integrated in the processor die. Intel Xeon processor 5600 series can support up to 3 channels of DDR3, DDR3L memory, with up to 3 DIMMs per channel. Please refer to Intel Plan of Record for supported DIMM types, densities and configurations.
- **Intel® Turbo Boost Technology** - A way to automatically run the processor core faster than the marked frequency if the part is operating under power, temperature, and current specification limits of the Thermal Design Power (TDP). This results in increased performance of both single and multi-threaded applications.

- **Intel® Trusted Execution Technology** - A highly versatile set of hardware extensions to Intel processors and chipsets that, with appropriate software, enhance the platform security capabilities.
- **Intel® QuickPath Interconnect (Intel® QPI)** — A cache-coherent, links-based interconnect specification for Intel processors, chipsets, and I/O bridge components.
- **Intel® 64 Architecture** — An enhancement to Intel's IA-32 architecture, allowing the processor to execute operating systems and applications written to take advantage of Intel® 64.
- **Intel® Virtualization Technology (Intel® VT)** — A set of hardware enhancements to Intel server and client platforms that can improve virtualization solutions. VT provides a foundation for widely-deployed virtualization solutions and enables more robust hardware assisted virtualization solution.
- **Integrated Heat Spreader (IHS)** — A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
- **Jitter** — Any timing variation of a transition edge or edges from the defined Unit Interval (UI).
- **LGA1366 Socket** — The 1366-land FC-LGA package mates with the system board through this surface mount, 1366-contact socket.
- **Network Equipment Building System (NEBS)** — The most common set of environmental design guidelines applied to telecommunications equipment in the United States.
- **Server SKU** — A processor Stock Keeping Unit (SKU) to be installed in either server or workstation platforms. Electrical, power and thermal specifications for these SKU's are based on specific use condition assumptions. Server processors may be further categorized as Frequency Optimized, Advanced, Standard and Low Power SKUs. For further details on use condition assumptions, please refer to the latest Product Release Qualification (PRQ) Report available via your Customer Quality Engineer (CQE) contact.
- **Storage Conditions** — Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor lands should not be connected to any supply voltages, have any I/Os biased, or receive any clocks.
- **Unit Interval (UI)** — Signaling convention that is binary and unidirectional. In this binary signaling, one bit is sent for every edge of the forwarded clock, whether it be a rising edge or a falling edge. If a number of edges are collected at instances t_1, t_2, t_n,...., t_k then the UI at instance "n" is defined as:

$$UI_n = t_n - t_{n-1}$$

- **Workstation SKU** — A processor SKU to be installed in workstation platforms only. Electrical, power and thermal specifications for these processors have been developed based on Intel's reliability goals at a reference use condition. In addition, the processor validation and production test conditions have been optimized based on these conditions. Operating "Workstation" processors in a server environment or other application, could impact reliability performance, which means Intel's reliability goals may not be met. For further details on use condition assumptions or reliability performance, please refer to the latest Product Release Qualification (PRQ) Report available via your Customer Quality Engineer (CQE) contact.



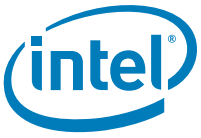
1.4 References

Platform designers are strongly encouraged to maintain familiarity with the most up-to-date revisions of processor and platform collateral.

Table 1-2. References

Document	Location / Document#[1]	Notes
Advanced Configuration and Power Interface Specification	www.acpi.info.	
Compact Electronics Bay Specification: A Server System Infrastructure (SSI) Specification for Value Servers and Workstations	www.ssiforum.org	
Electronics Bay Specification for 2008 Servers and Workstation		
Entry-Level Electronics-Bay Specifications: A Server System Infrastructure (SSI) Specification for Entry Pedestal Servers and Workstations		
Thin Electronics Bay Specification: A Server System Infrastructure (SSI) Specification for Rack-Optimized Servers		
Intel® 64 and IA-32 Architecture Software Developer's Manual • *Volume 1: Basic Architecture* • *Volume 2A: Instruction Set Reference, A-M* • *Volume 2B: Instruction Set Reference, N-Z* • *Volume 3A: System Programming Guide, Part 1* • *Volume 3B: Systems Programming Guide, Part 2*	 253665 253666 253667 253668 253669	1
Intel® 64 and IA-32 Architectures Optimization Reference Manual	248966	1
Intel® Xeon® Processor 5600 Series Datasheet, Volume 2	323370	1
Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines	323371	1

Notes:
1. Document is available publicly at http://www.intel.com.



2 Electrical Specifications

2.1 Processor Signaling

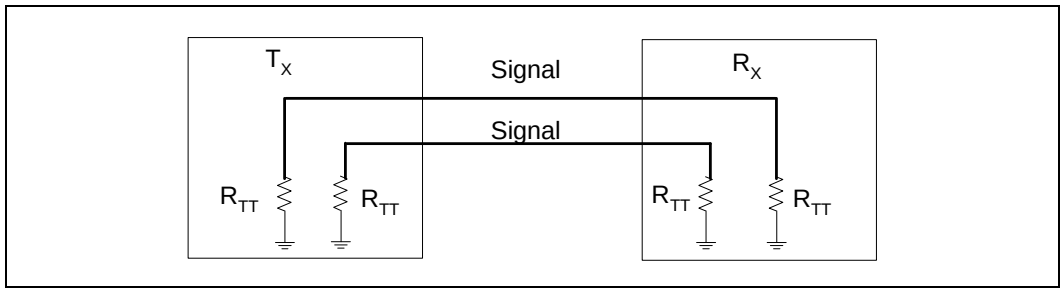
The Intel Xeon processor 5600 series include 1366 lands, which utilize various signaling technologies. Signals are grouped by electrical characteristics and buffer type into various signal groups. These include Intel® QuickPath Interconnect, DDR3 (Reference Clock, Command, Control, and Data), Platform Environmental Control Interface (PECI), Processor Sideband, System Reference Clock, Test Access Port (TAP), and Power/Other signals. Refer to Table 2-5 for details.

2.1.1 Intel® QuickPath Interconnect

The Intel Xeon processor 5600 series provide two Intel® QuickPath Interconnect ports for high speed serial transfer between other enabled components. Each port consists of two uni-directional links (for transmit and receive). A differential signaling scheme is utilized, which consists of opposite-polarity (D_P, D_N) signal pairs.

On-die termination (ODT) is included on the processor silicon and terminated to V_{SS}. Intel chipsets also provide ODT, thus eliminating the need to terminate on the system board. Figure 2-1 illustrates the active ODT.

Figure 2-1. Active ODT for a Differential Link Example



2.1.2 DDR3 Signal Groups

The memory interface utilizes DDR3 technology, which consists of numerous signal groups. These include: Reference Clocks, Command Signals, Control Signals, and Data Signals. Each group consists of numerous signals, which may utilize various signaling technologies. Please refer to Table 2-5 for further details.

2.1.3 Platform Environmental Control Interface (PECI)

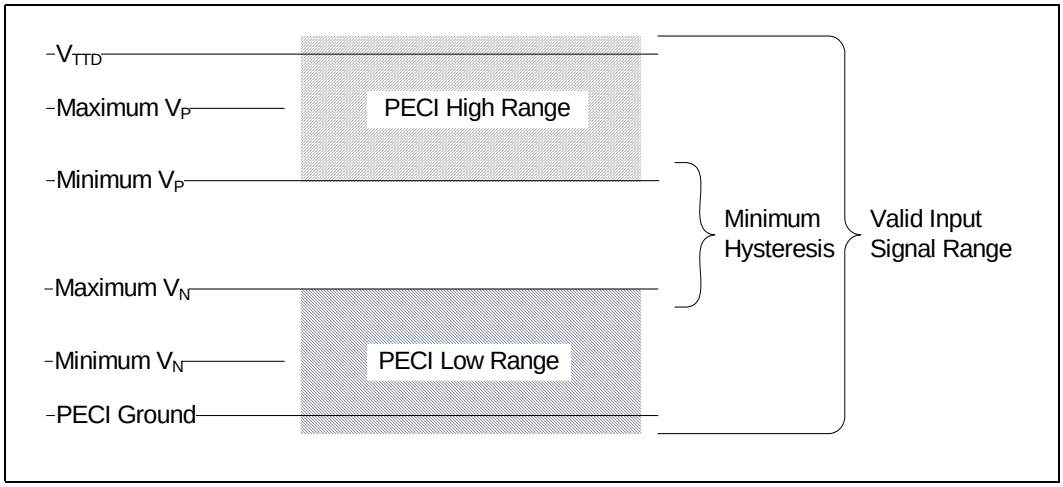
PECI is an Intel proprietary interface that provides a communication channel between Intel processors and chipset components to external thermal monitoring devices. The processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read processor temperature, perform processor manageability functions, and manage processor interface tuning and diagnostics. Please refer to Section 7.3 for processor specific implementation details for PECI.

The PECI interface operates at a nominal voltage set by V_{TTD}. The set of DC electrical specifications shown in Table 2-13 is used with devices normally operating from a V_{TTD} interface supply.

2.1.3.1 Input Device Hysteresis

The PECI client and host input buffers must use a Schmitt-triggered input design for improved noise immunity. Please refer to Figure 2-2 and Table 2-13.

Figure 2-2. Input Device Hysteresis



2.1.4 Processor Sideband Signals

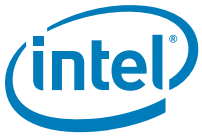
Intel Xeon processor 5600 series include sideband signals that provide a variety of functions. Details can be found in Table 2-5.

All Asynchronous Processor Sideband signals are required to be asserted/deasserted for at least eight BCLKs in order for the processor to recognize the proper signal state. See Table 2-18 and Table 2-26 for DC and AC specifications, respectively. Refer to Section 3 for applicable signal integrity specifications.

2.1.5 System Reference Clock

The processor core, processor uncore, Intel QuickPath Interconnect link, and DDR3 memory interface frequencies are generated from BCLK_DP and BCLK_DN signals. There is no direct link between core frequency and Intel QuickPath Interconnect link frequency (e.g., no core frequency to Intel QuickPath Interconnect multiplier). The processor maximum core frequency, Intel QuickPath Interconnect link frequency and DDR memory frequency are set during manufacturing. It is possible to override the processor core frequency setting using software. This permits operation at lower core frequencies than the factory set maximum core frequency.

The processor core frequency is configured during reset by using values stored within the device during manufacturing. The stored value sets the lowest core multiplier at which the particular processor can operate. If higher speeds are desired, the appropriate ratio can be configured via the IA32_PERF_CTL MSR (MSR 199h); Bits [15:0].



Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK_DP, BCLK_DN input, with exceptions for spread spectrum clocking. DC specifications for the BCLK_DP, BCLK_DN inputs are provided in Table 2-14 and AC specifications in Table 2-22. These specifications must be met while also meeting the associated signal quality specifications outlined in Section 3.

2.1.6 Test Access Port (TAP) Signals

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the processor(s) be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Similar considerations must be made for TCK, TDO, TMS, and TRST#. Two copies of each signal may be required with each driving a different voltage level.

Processor TAP signal DC specifications can be found in Table 2-18. AC specifications are located in Table 2-27.

Note: While TDI, TMS and TRST# do not include On-Die Termination (ODT), these signals are weakly pulled-up via a 1-5 kΩ resistor to V_{TT}.

Note: While TCK does not include ODT, this signal is weakly pulled-down via a 1-5 kΩ resistor to V_{SS}.

2.1.7 Power / Other Signals

Processors also include various other signals including power/ground, sense points, and analog inputs. Details can be found in Table 2-5.

Table 2-1 outlines the required voltage supplies necessary to support Intel Xeon processor 5600 series.

Table 2-1. Processor Power Supply Voltages[1]

Power Rail	Nominal Voltage	Notes
V_{CC}	See Table 2-9; Figure 2-3	Each processor includes a dedicated VR11.1 regulator.
V_{CCPLL}	1.80 V	Each processor includes dedicated V_{CCPLL} and PLL circuits.
V_{DDQ}	1.50 V 1.35 V	Each processor and DDR3 / DDR3L stack shares a dedicated voltage regulator. It is expected that regulators will support both 1.50 and 1.35 V.
V_{TTA}, V_{TTD}	See Table 2-11; Figure 2-10	Each processor includes a dedicated VR11.0 regulator. $V_{TT} = V_{TTA} + V_{TTD}$; P1V1_Vtt is VID[4:2] controlled, VID range is 1.025-1.2000V; 20 mV offset (see Table 2-4); V_{TT} represents a ***typical*** voltage. V_{TT_MIN} and V_{TT_MAX} loadlines represent a 31.5 mV offset from V_{TT} (typ).

Note:
1. Refer to Table 2-8 for voltage and current specifications.

2.1.7.1 Power and Ground Lands

For clean on-chip power distribution, processors include lands for all required voltage supplies. These include:

- 210 each V_{CC} (271 ea. V_{SS}) lands must be supplied with the voltage determined by the VID[7:0] signals. Table 2-2 defines the voltage level associated with each core VID pattern. Table 2-9 and Figure 2-3 represent V_{CC} static and transient limits.
- 3 each V_{CCPLL} lands, connected to a 1.8 V supply, power the Phase Lock Loop (PLL) clock generation circuitry. An on-die PLL filter solution is implemented within the processor.
- 45 each V_{DDQ} (17 ea. V_{SS}) lands, connected to a 1.50 / 1.35 V supply, provide power to the processor DDR3 interface. This supply also powers the DDR3 memory subsystem.
- 7 each V_{TTA} (5 ea. V_{SS}) and 26 ea. V_{TTD} (17 ea. V_{SS}) lands must be supplied with the voltage determined by the VTT_VID[4:2] signals. Coupled with a 20 mV offset, this corresponds to a VTT_VID pattern of '010xxx10'. Table 2-4 specifies the voltage levels associated with each VTT_VID pattern. Table 2-11 and Figure 2-10 represent V_{TT} static and transient limits.

All V_{CC}, V_{CCPLL}, V_{DDQ}, V_{TTA}, and V_{TTD} lands must be connected to their respective processor power planes, while all V_{SS} lands must be connected to the system ground plane.

2.1.7.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic capacitors, supply

current during longer lasting changes in current demand, for example coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition. Care must be taken in the baseboard design to ensure that the voltages provided to the processor remain within the specifications listed in Table 2-8. Failure to do so can result in timing violations or reduced lifetime of the processor.

2.1.7.3 Processor V_{CC} Voltage Identification (VID) Signals

The voltage set by the VID signals is the maximum reference voltage regulator (VR) output to be delivered to the processor V_{CC} lands. VID signals are CMOS push/pull outputs. Please refer to Table 2-18 for the DC specifications for these signals.

Individual processor VID values may be calibrated during manufacturing such that two devices at the same core frequency may have different default VID settings.

The processor uses eight voltage identification signals, VID[7:0], to support automatic selection of power supply voltages. Table 2-2 specifies the voltage level corresponding to the state of VID[7:0]. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. If the processor socket is empty (SKTOCC# pulled high), or the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself.

The processor provides the ability to operate while transitioning to an adjacent VID and its associated processor core voltage (V_{CC}). This is represented by a DC shift in the loadline. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target core voltage. Transitions above the maximum specified VID are not permitted. Table 2-8 includes VID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 2-9.

The VRM or EVRD utilized must be capable of regulating its output to the value defined by the new VID. DC specifications for dynamic VID transitions are included in Table 2-18, while AC specifications are included in Table 2-28.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

Table 2-2. Voltage Identification Definition (Sheet 1 of 6)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375

Table 2-2. Voltage Identification Definition (Sheet 2 of 6)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125

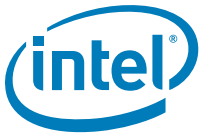


Table 2-2. Voltage Identification Definition (Sheet 3 of 6)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875

Table 2-2. Voltage Identification Definition (Sheet 4 of 6)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625

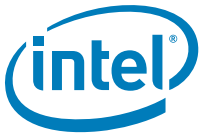


Table 2-2. Voltage Identification Definition (Sheet 5 of 6)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625

Table 2-2. Voltage Identification Definition (Sheet 6 of 6)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

Notes:
1. When the "11111111" VID pattern is observed, or when the SKTOCC# pin is pulled high, the voltage regulator output should be disabled.
2. The VID range includes VID transitions that may be initiated by thermal events, Extended HALT state transitions (see Section 8.2), higher C-States (see Section 8.2) or Enhanced Intel SpeedStep® Technology transitions (see Section 8.5). **The Extended HALT state must be enabled for the processor to remain within its specifications**
3. Once the VRM/EVRD is operating after power-up, if either the Output Enable signal is de-asserted or a specific VID off code is received, the VRM/EVRD must turn off its output (the output should go to high impedance) within 500 ms and latch off until power is cycled.

2.1.7.3.1 Power-On Configuration (POC) Logic

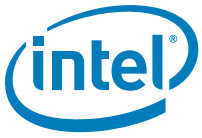
VID[7:0] signals also serve a second function. During power-up, Power-On Configuration POC[7:0] logic levels are MUX'ed onto these signals via 1-5 kΩ pull-up or pull down resistors located on the baseboard. These values provide voltage regulator keying (VID[7]), inform the processor of the platforms power delivery capabilities (MSID[2:0]), and program the gain applied to the ISENSE input (CSC[2:0]). Table 2-3 maps VID signals to the corresponding POC functionality.

Table 2-3. Power-On Configuration (POC[7:0]) Decode

Function	Bits	POC Settings		Description
VR_Key	VID[7]	0b for VR11.1		Electronic safety key distinguishing VR11.1
Spare	VID[6]	0b (default)		Reserved for future use
CSC[2:0]	VID[5:3]	-000b -001b -010b -011b -100b -101b -111b	Feature Disabled ICC_MAX = 40 A[1] 40 W TDP / ICC_MAX = 50 A 60 W TDP / ICC_MAX = 80 A 80W TDP / ICC_MAX = 100 A 95W TDP / ICC_MAX = 120 A 130W TDP / ICC_MAX = 150A[2]	Current Sensor Configuration (CSC) programs the gain applied to the ISENSE A/D output. ISENSE data is then used to dynamically calculate current and power.
MSID[2:0]	VID[2:0]	-001b -011b -100b -101b -110b	40 W TDP / 50 A ICC_MAX 60 W TDP / 80 A ICC_MAX 80 W TDP / 100 A ICC_MAX 95 W TDP / 120 A ICC_MAX 130 W TDP / 150 A ICC_MAX	MSID[2:0] signals are provided to indicate the Market Segment for the processor and may be used for future processor compatibility or keying. See Section 8.1 for platform timing requirements of the MSID[2:0] signals.

Note:
1. This setting is defined for future use; no Intel Xeon processor 5600 series SKU is defined with ICC_MAX=40 A.
2. In general, set PWM IMON slope to 900 mV = IMAX, where IMAX = ICCMAX. For the 130 W SKU, set IMON slope to 900 mV= 180 A. All other SKUs must match the values shown above. Please consult the PWM datasheet for the IMON slope setting.

Some POC signals include specific timing requirements. Please refer to Section 8.1 for further details.



2.1.7.4 Processor V_{TT} Voltage Identification (VTT_VID) Signals

The voltage set by the VTT_VID signals is the typical reference voltage regulator (VR) output to be delivered to the processor V_{TTA} and V_{TTD} lands. It is expected that one regulator will supply all V_{TTA} and V_{TTD} lands. VTT_VID signals are CMOS push/pull outputs. Please refer to Table 2-18 for the DC specifications for these signals.

Individual processor VTT_VID values may be calibrated during manufacturing such that two devices at the same core frequency may have different default VTT_VID settings.

The processor utilizes three voltage identification signals to support automatic selection of power supply voltages. These correspond to VTT_VID[4:2]. The V_{TT} voltage level delivered to the processor lands must also encompass a 20 mV offset (See Table 2-4; V_{TT_TYP}) above the voltage level corresponding to the state of the VTT_VID[7:0] signals (See Table 2-4; VR 11.0 Voltage). Table 2-11 and Figure 2-10 provide the resulting static and transient tolerances. Please note that the maximum and minimum electrical loadlines are defined by a 31.5 mV tolerance band above and below V_{TT_TYP} values.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

Table 2-4. V_{TT} Voltage Identification Definition

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VR 11.0 Voltage	V_{TT_TYP} (Voltage + Offset)
0	1	0	0	0	0	1	0	1.200V	1.220V
0	1	0	0	0	1	1	0	1.175V	1.195V
0	1	0	0	1	0	1	0	1.150V	1.170V
0	1	0	0	1	1	1	0	1.125V	1.145V
0	1	0	1	0	0	1	0	1.100V	1.120V
0	1	0	1	0	1	1	0	1.075V	1.095V
0	1	0	1	1	0	1	0	1.050V	1.070V
0	1	0	1	1	1	1	0	1.025V	1.045V

2.1.8 Reserved or Unused Signals

All Reserved (RSVD) signals must remain unconnected. Connection of these signals to V_{CC}, V_{TTA}, V_{TTD}, V_{DDQ}, V_{SS}, or any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Section 5 for the land listing and the location of all Reserved signals.

For reliable operation, connect unused inputs or bidirectional signals to an appropriate signal level. Unused Intel® QuickPath Interconnect input and output pins can be left floating. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected; however, this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, including a resistor will also allow for system testability. Resistor values should be within ± 20% of the impedance of the baseboard trace, unless otherwise noted in the appropriate platform design guidelines.

TAP signals do not include on-die termination, however they may include resistors on package (refer to Section 2.1.6 for details). Inputs and utilized outputs must be terminated on the baseboard. Unused outputs may be terminated on the baseboard or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing.

2.2 Signal Group Summary

Signals are aligned in Table 2-5 by buffer type and characteristics. “Buffer Type” denotes the applicable signaling technology and specifications.

Table 2-5. Signal Groups (Sheet 1 of 2)

Signal Group	Buffer Type	Signals[1]
Intel® QuickPath Interconnect Signals		
Differential	Intel® QuickPath Interconnect Input	QPI[0/1]_DRX_D[N/P][19:0], QPI[0/1]_CLKRX_DP, QPI[0/1]_CLKRX_DN
Differential	Intel® QuickPath Interconnect Output	QPI[0/1]_DTX_D[N/P][19:0], QPI[0/1]_CLKTX_DP, QPI[0/1]_CLKTX_DN
Single ended	Analog Input	QPI[0/1]_COMP
DDR3 Reference Clocks[2]		
Differential	Output	DDR{0/1/2}_CLK_[P/N][3:0]
DDR3 Command Signals[2]		
Single ended	CMOS Output	DDR{0/1/2}_RAS#, DDR{0/1/2}_CAS#, DDR{0/1/2}_WE#, DDR{0/1/2}_MA[15:0], DDR{0/1/2}_BA[2:0], DDR{0/1/2}_MA_PAR
	Asynchronous Output	DDR{0/1/2}_RESET#
DDR3 Control Signals[2]		
Single ended	CMOS Output	DDR{0/1/2}_CS#[7:0], DDR{0/1/2}_ODT[5:0], DDR{0/1/2}_CKE[3:0]
Single ended	Analog Input	DDR_VREF, DDR_COMP[2:0]
DDR3 Data Signals[2]		
Single ended	CMOS Input/Output	DDR{0/1/2}_DQ[63:0], DDR{0/1/2}_ECC[7:0]
Differential	CMOS Input/Output	DDR{0/1/2}_DQS_[N/P][17:0]
Single ended	Asynchronous Input	DDR{0/1/2}_PAR_ERR#[2:0], DDR_THERM#, DDR_THERM2#
Platform Environmental Control Interface (PECI)		
Single ended	Asynchronous Input/Output	PECI
Processor Sideband Signals		
Single ended	GTL Input/Output	BPM#[7:0], CAT_ERR#
Single ended	Asynchronous Input	PECI_ID#
Single ended	Asynchronous GTL Output	PRDY#, THERMTRIP#
Single ended	Asynchronous GTL Input	PREQ#
Single ended	Asynchronous GTL Input/Output	PROCHOT#
Single ended	Asynchronous CMOS Output	PSI#, TAPPWRGOOD
Single ended	CMOS Output	VID[7:6], VID[5:3]/CSC[2:0], VID[2:0]/MSID[2:0], VTT_VID[4:2]
PWRGOOD Signal		
Single ended	Asynchronous Input	VCCPWRGOOD, VDDPWRGOOD, VTTPWRGOOD
Reset Signal		
Single ended	Reset Input	RESET#

Table 2-5. Signal Groups (Sheet 2 of 2)

Signal Group	Buffer Type	Signals[1]
System Reference Clock		
Differential	Input	BCLK_DP, BCLK_DN
Test Access Port (TAP) Signals		
Differential	CMOS Output	BCLK_ITP_DP, BCLK_ITP_DN
Single ended	Input	TCK, TDI, TMS, TRST#
Single ended	GTL Output	TDO
Power/Other Signals		
	Power / Ground	V_{CC}, V_{CCPLL}, V_{DDQ}, V_{TTA}, V_{TTD}, V_{SS}
	Analog Input	COMP0, ISENSE
	Sense Points	VCCSENSE, VSSSENSE, VSS_SENSE_VTTD, VTTD_SENSE
	Other	SKTOCC#, DBR#

Notes:
1. Refer to Section 5 for land assignments and Section 6 for signal definitions.
2. DDR{0/1/2} refers to DDR3 channel 0, DDR3 channel 1, and DDR3 Channel 2

Signals that include on-die termination (ODT) are listed in Table 2-6.

Table 2-6. Signals With On-Die Termination (ODT)

Intel® QuickPath Interface Signal Group[1]
QPI[1:0]_DRX_DP[19:0], QPI[1:0]_DRX_DN[19:0], QPI[1:0]_TRX_DP[19:0], QPI[1:0]_TRX_DN[19:0], QPI[0/1]_CLKRX_D[N/P], QPI[0/1]_CLKTX_D[N/P]
DDR3 Signal Group[1,2]
DDR{0/1/2}_DQ[63:0], DDR{0/1/2}_DQS_[N/P][17:0], DDR{0/1/2}_ECC[7:0], DDR{0/1/2}_PAR_ERR#[2:0][3]
Processor Sideband Signal Group[1]
BPM#[7:0][6], PECI_ID#[7], PREQ#[6], TAPPWRGOOD[8]
Test Access Port (TAP) Signal Group
TCK[4], TDI[5], TMS[5], TRST#[5]
Power/Other Signal Group[9]
TAPPWRGOOD[8], VCCPWRGOOD, VDDPWRGOOD, VTTPWRGOOD

Notes:
1. Unless otherwise specified, signals have ODT in the package with a 50 Ω pull-down to V_{SS}.
2. Unless otherwise specified, all DDR3 signals are terminated to $V_{DDQ}/2$.
3. DDR{0/1/2}_PAR_ERR#[2:0] are terminated to V_{DDQ}.
4. TCK does not include ODT, this signal is weakly pulled-down via a 1-5 kΩ resistor to V_{SS}.
5. TDI, TMS, TRST# do not include ODT, these signals are weakly pulled-up via 1-5kΩ resistor to V_{TT}.
6. BPM[7:0]# and PREQ# signals have ODT in package with 35 Ω pull-ups to V_{TT}.
7. PECI_ID# has ODT in package with a 1-5 kΩ pull-up to V_{TT}.
8. TAPPWRGOOD has ODT in package with a 1-2.5 kΩ pull-up to V_{TT}.
9. VCCPWRGOOD, VDDPWRGOOD, and VTTPWRGOOD have ODT in package with a 5-20 kΩ pull-down to V_{SS}.

2.3 Mixing Processors

Intel supports dual-processor (DP) configurations consisting of processors:

- from the same power optimization segment.
- that support the same maximum Intel® QuickPath Interconnect and DDR3 memory speeds.

- that share symmetry across physical packages with respect to the number of logical processor per package, number of cores per package, number of Intel® QuickPath interfaces, and cache topology.
- that have identical Extended Family, Extended Model, Processor Type, Family Code and Model Number as indicated by the Function 1 of the CPUID instruction.

Note: Processors must operate with the same Intel® QuickPath Interconnect, DDR3 memory and core frequency.

While Intel does nothing to prevent processors from operating together, some combinations may not be supported due to limited validation, which may result in uncharacterized errata. Coupling this fact with the large number of Intel® Xeon® 5600 series processor attributes, the following population rules and stepping matrix have been developed to clearly define supported configurations.

- Processors must be of the same power-optimization segment. This insures processors include the same maximum Intel® QuickPath Interconnect and DDR3 operating speeds and cache sizes.
- Processors must operate at the same core frequency. Note, processors within the same power-optimization segment supporting different maximum core frequencies can be operated within a system. However, both must operate at the highest frequency rating commonly supported. Mixing components operating at different internal clock frequencies is not supported and will not be validated by Intel.
- Processors must share symmetry across physical packages with respect to the number of logical processors per package, number of cores per package (but not necessarily the same subset of cores within the packages), number of Intel® QuickPath interfaces and cache topology.
- Mixing steppings is only supported with processors that have identical Extended Family, Extended Model, Processor Type, Family Code and Model Number as indicated by the Function 1 of the CPUID instruction. Mixing processors of different steppings, but the same mode (as per CPUID instruction) is supported. Details regarding the CPUID instruction are provide in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A*.
- After AND'ing the feature flag and extended feature flags from the installed processors, any processor whose set of feature flags exactly matches the AND'ed feature flags can be selected by the BIOS as the BSP. If no processor exactly matches the AND'ed feature flag values, then the processor with the numerically lower CPUID should be selected as the BSP.
- Intel requires that the proper microcode update be loaded on each processor operating within the system. Any processor that does not have the proper microcode update loaded is considered by Intel to be operating out-of-specification.
- Customers are fully responsible for the validation of their system configurations

Note: Processors within a system must operate at the same frequency per bits [15:8] of the FLEX_RATIO MSR (Address: 194h); however this does not apply to frequency transitions initiated due to thermal events, Extended HALT, Enhanced Intel SpeedStep Technology transitions signal (See Section 8).

2.4 Flexible Motherboard Guidelines (FMB)

The Flexible Motherboard (FMB) guidelines are estimates of the maximum values the processor will have over certain time periods. The values are only estimates and actual specifications for future processors may differ. Processors may or may not have

specifications equal to the FMB value in the foreseeable future. System designers should meet the FMB values to ensure their systems will be compatible with future processors.

2.5 Absolute Maximum and Minimum Ratings

Table 2-7 specifies absolute maximum and minimum ratings only, which lie outside the functional limits of the processor. Only within specified operation limits, can functionality and long-term reliability be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 2-7. Processor Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1,2]
V_{CC}	Processor core voltage with respect to V_{SS}	-0.3	1.4	V	
V_{CCPLL}	Processor PLL voltage with respect to V_{SS}	-0.3	2.0	V	4
V_{DDQ}	Processor I/O supply voltage for DDR3 with respect to V_{SS}	-0.3	1.8	V	4
V_{TTA}	Processor uncore analog voltage with respect to V_{SS}	-0.3	1.4	V	3
V_{TTD}	Processor uncore digital voltage with respect to V_{SS}	-0.3	1.4	V	3
T_{CASE}	Processor case temperature	See Section 7	See Section 7	°C	
$T_{STORAGE}$	Storage temperature	See Section 7.4	See Section 7.4	°C	5,6,7
V_{ISENSE}	Analog input voltage with respect to VSS for sensing core current consumption	-0.3	1.15	V	

Notes:
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in Section 3. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. V_{TTA} and V_{TTD} should be derived from the same voltage regulator (VR).
4. 5% tolerance
5. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specification.
6. This rating applies to the processor and does not include any tray or packaging.
7. Failure to adhere to this specification can affect the long-term reliability of the processor

2.6 Processor DC Specifications

DC specifications are defined at the processor pads, unless otherwise noted. DC specifications are only valid while meeting specifications for case temperature (T_{CASE} specified in **Section 7, "Thermal Specifications"**), clock frequency, and input voltages. Care should be taken to read all notes associated with each specification.

Table 2-8. Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Voltage Plane	Min	Typ	Max	Unit	Notes[1]
VID	V_{CC} VID Range	-	0.750		1.350	V	2,3
V_{CC}	Core Voltage (Launch - FMB)	V_{CC}	V_{CCMAX}=VID-(I_{CC} * 0.8 mΩ) V_{CCMIN}=(VID-VRTOL)-(I_{CC}*0.8 mΩ) See Table 2-9 and Figure 2-3			V	3,4,6,7,11
V_{VID_STEP}	VID step size during a transition	-			±6.250	mV	9
V_{CCPLL}	PLL Voltage (DC + AC specification)	V_{CCPLL}	0.95*V_{CCPLL} (Typ)	1.800	1.05*V_{CCPLL} (Typ)	V	10
V_{DDQ}	I/O Voltage for DDR3 (DC + AC specification)	V_{DDQ}	0.95*V_{DDQ} (Typ)	1.500	1.05*V_{DDQ} (Typ)	V	10
V_{DDQ}	I/O Voltage for DDR3L (DC + AC specification)	V_{DDQ}	0.95*V_{DDQ} (Typ)	1.350	1.075*V_{DDQ} (Typ)	V	10
VTT_VID	V_{TT} VID Range	-	1.045		1.220	V	2,3
V_{TT}	Uncore Voltage (Launch - FMB)	V_{TT}	V_{TT_TYP}=VTT_VID-(I_{TT}*6 mΩ) V_{TT_MAX}=V_{TTTYP} + 31.5 mV V_{TT_MIN}=V_{TTTYP} - 31.5 mV See Table 2-11 and Figure 2-10			V	3,5,8,11
I_{CC_MAX} I_{CCPLL_MAX} I_{DDQ_MAX} I_{TT_MAX}	Max. Processor Current: Frequency Optimized Server/Workstation (TDP = 130 W) (Launch - FMB)	V_{CC} V_{CCPLL} V_{DDQ} V_{TTA} V_{TTD}			150 1.1 9 6 22	A A A A A	11
	Max. Processor Current: Advanced Server/Workstation (TDP = 95 W) (Launch - FMB)	V_{CC} V_{CCPLL} V_{DDQ} V_{TTA} V_{TTD}			120 1.1 9 6 22	A A A A A	11
	Max. Processor Current: Standard Server/Workstation (TDP = 80 W) (Launch - FMB)	V_{CC} V_{CCPLL} V_{DDQ} V_{TTA} V_{TTD}			100 1.1 9 6 22	A A A A A	11
	Max. Processor Current: Low Power & LV-60W (TDP = 60 W) (Launch - FMB)	V_{CC} V_{CCPLL} V_{DDQ} V_{TTA} V_{TTD}			80 1.1 9 6 20	A A A A A	11
	Max. Processor Current: Low Power & LV-40W (TDP = 40 W) (Launch - FMB)	V_{CC} V_{CCPLL} V_{DDQ} V_{TTA} V_{TTD}			50 1.1 9 6 20	A A A A A	11

Table 2-8. Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Voltage Plane	Min	Typ	Max	Unit	Notes[1]
I_{CC_TDC} I_{CCPLL_TDC} I_{DDQ_TDC} I_{TT_TDC}	Thermal Design Current: Frequency Optimized Server/Workstation (TDP = 130 W) (Launch - FMB)	V_{CC} V_{CCPLL} V_{DDQ} V_{TTA} V_{TTD}			110 1.1 9 6 22	A A A A A	11,12
	Thermal Design Current: Advanced Server/Workstation (TDP = 95 W) (Launch - FMB)	V_{CC} V_{CCPLL} V_{DDQ} V_{TTA} V_{TTD}			101 1.1 9 6 22	A A A A A	11,12
	Thermal Design Current: Standard Server/Workstation (TDP = 80 W) (Launch - FMB)	V_{CC} V_{CCPLL} V_{DDQ} V_{TTA} V_{TTD}			70 1.1 9 6 22	A A A A A	11,12
	Thermal Design Current: Low Power & LV-60W (TDP = 60 W) (Launch - FMB)	V_{CC} V_{CCPLL} V_{DDQ} V_{TTA} V_{TTD}			60 1.1 9 6 20	A A A A A	11,12
	Thermal Design Current: Low Power & LV-40W (TDP = 40 W) (Launch - FMB)	V_{CC} V_{CCPLL} V_{DDQ} V_{TTA} V_{TTD}			40 1.1 9 6 20	A A A A A	11,12
I_{DDQ_S3}	DDR3 System Memory Interface Supply Current in Standby State	V_{DDQ}			1	A	13,14

Notes:

1. Unless otherwise noted, all specifications in this table apply to all processors.
2. Individual processor VID and/or VTT_VID values may be calibrated during manufacturing such that two devices at the same speed may have different settings.
3. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required.
4. The V_{CC} voltage specification requirements are measured across vias on the platform for the VCCSENSE and VSSSENSE pins close to the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
5. The V_{TT} voltage specification requirements are measured across vias on the platform for the VTTD_SENSE and VSS_SENSE_VTTD lands close to the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
6. Refer to Table 2-9 and corresponding Figure 2-3. The processor should not be subjected to any static V_{CC} level that exceeds the V_{CC_MAX} associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
7. Minimum V_{CC} and maximum I_{CC} are specified at the maximum processor case temperature (T_{CASE}) shown in Table 7-1. I_{CC_MAX} is specified at the relative V_{CC_MAX} point on the V_{CC} load line. The processor is capable of drawing I_{CC_MAX} for up to 10 ms. Refer to Figure 2-5 through Figure 2-8 for further details on the average processor current draw over various time durations.
8. Refer to Table 2-11 and corresponding Figure 2-10. The processor should not be subjected to any static V_{TT} level that exceeds the V_{TT_MAX} associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
9. This specification represents the V_{CC} reduction due to each VID transition. See Section 2.1.7.3. AC timing requirements for VID transitions are included in Figure 2-29.
10. Baseboard bandwidth is limited to 20 MHz.
11. FMB is the flexible motherboard guidelines. See Section 2.4 for FMB details.
12. ICC_TDC (Thermal Design Current) is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and should be used for the voltage regulator temperature assessment. The voltage regulator is responsible for monitoring its temperature and asserting the necessary signal to inform the processor of a thermal excursion.

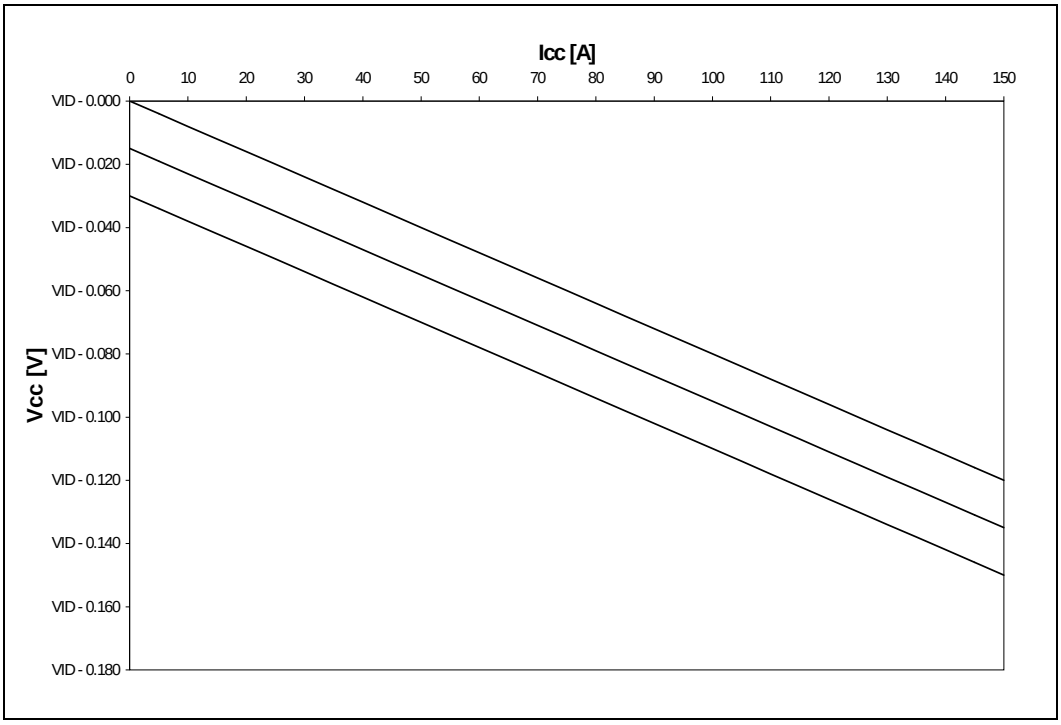
13. Specification is at T_{CASE} = 50 °C.
14. Characterized by design (not tested)

Table 2-9. V_{CC} Static and Transient Tolerance

I_{CC} (A)	V_{CC_MAX} (V)	V_{CC_TYP} (V)	V_{CC_MIN} (V)	Notes[1,2,3,4]
0	VID - 0.000	VID - 0.015	VID - 0.030	
5	VID - 0.004	VID - 0.019	VID - 0.034	
10	VID - 0.008	VID - 0.023	VID - 0.038	
15	VID - 0.012	VID - 0.027	VID - 0.042	
20	VID - 0.016	VID - 0.031	VID - 0.046	
25	VID - 0.020	VID - 0.035	VID - 0.050	
30	VID - 0.024	VID - 0.039	VID - 0.054	
35	VID - 0.028	VID - 0.043	VID - 0.058	
40	VID - 0.032	VID - 0.047	VID - 0.062	
45	VID - 0.036	VID - 0.051	VID - 0.066	
50	VID - 0.040	VID - 0.055	VID - 0.070	
55	VID - 0.044	VID - 0.059	VID - 0.074	
60	VID - 0.048	VID - 0.063	VID - 0.078	
65	VID - 0.052	VID - 0.067	VID - 0.082	
70	VID - 0.056	VID - 0.071	VID - 0.086	
75	VID - 0.060	VID - 0.075	VID - 0.090	
80	VID - 0.064	VID - 0.079	VID - 0.094	
85	VID - 0.068	VID - 0.083	VID - 0.098	
90	VID - 0.072	VID - 0.087	VID - 0.102	
95	VID - 0.076	VID - 0.091	VID - 0.106	
100	VID - 0.080	VID - 0.095	VID - 0.110	
105	VID - 0.084	VID - 0.099	VID - 0.114	
110	VID - 0.088	VID - 0.103	VID - 0.118	
115	VID - 0.092	VID - 0.107	VID - 0.122	
120	VID - 0.096	VID - 0.111	VID - 0.126	
125	VID - 0.100	VID - 0.115	VID - 0.130	
130	VID - 0.104	VID - 0.119	VID - 0.134	
135	VID - 0.108	VID - 0.123	VID - 0.138	
140	VID - 0.112	VID - 0.127	VID - 0.142	
145	VID - 0.116	VID - 0.131	VID - 0.146	
150	VID - 0.120	VID - 0.135	VID - 0.150	

Notes:
1. The V_{CC_MIN} and V_{CC_MAX} loadlines represent static and transient limits. Please see Section 2.6.1 for V_{CC} overshoot specifications.
2. This table is intended to aid in reading discrete points on Figure 2-3.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCC_SENSE and VSS_SENSE lands.
4. Processor core current (I_{CC}) ranges are valid up to I_{CC_MAX} of the processor SKU as defined in Table 2-8.

Figure 2-3. V_{CC} Static and Transient Tolerance Loadlines[1,2,3,4]



Notes:
1. The V_{CC_MIN} and V_{CC_MAX} loadlines represent static and transient limits. Please see Section 2.6.1 for V_{CC} overshoot specifications.
2. Refer to Table 2-9 for V_{CC} Static and Transient Tolerance.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCC_SENSE and VSS_SENSE lands.
4. Processor core current (I_{CC}) ranges are valid up to I_{CC_MAX} of the processor SKU as defined in Table 2-8.

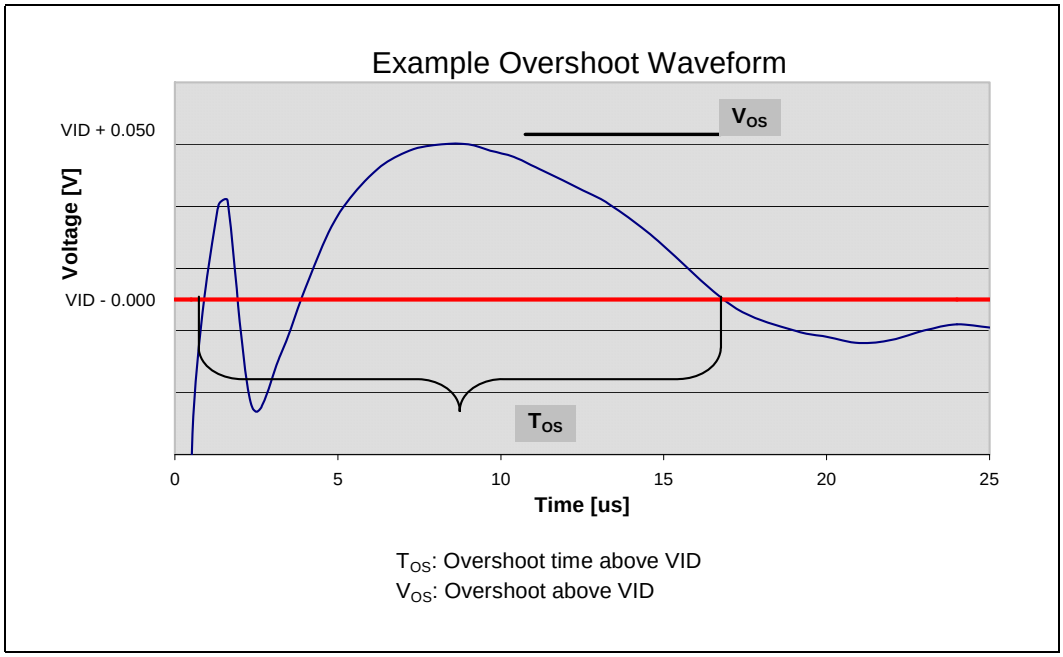
2.6.1 V_{CC} Overshoot Specifications

The processor can tolerate short transient overshoot events where V_{CC} exceeds the VID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed VID + V_{OS_MAX} (V_{OS_MAX} is the maximum allowable overshoot above VID). These specifications apply to the processor die voltage as measured across the VCC_SENSE and VSS_SENSE lands.

Table 2-10. V_{CC} Overshoot Specifications

Symbol	Parameter	Min	Max	Units	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CC} overshoot above VID	-	50	mV	2-4	
T_{OS_MAX}	Time duration of V_{CC} overshoot above VID	-	25	µs	2-4	

Figure 2-4. V_{CC} Overshoot Example Waveform

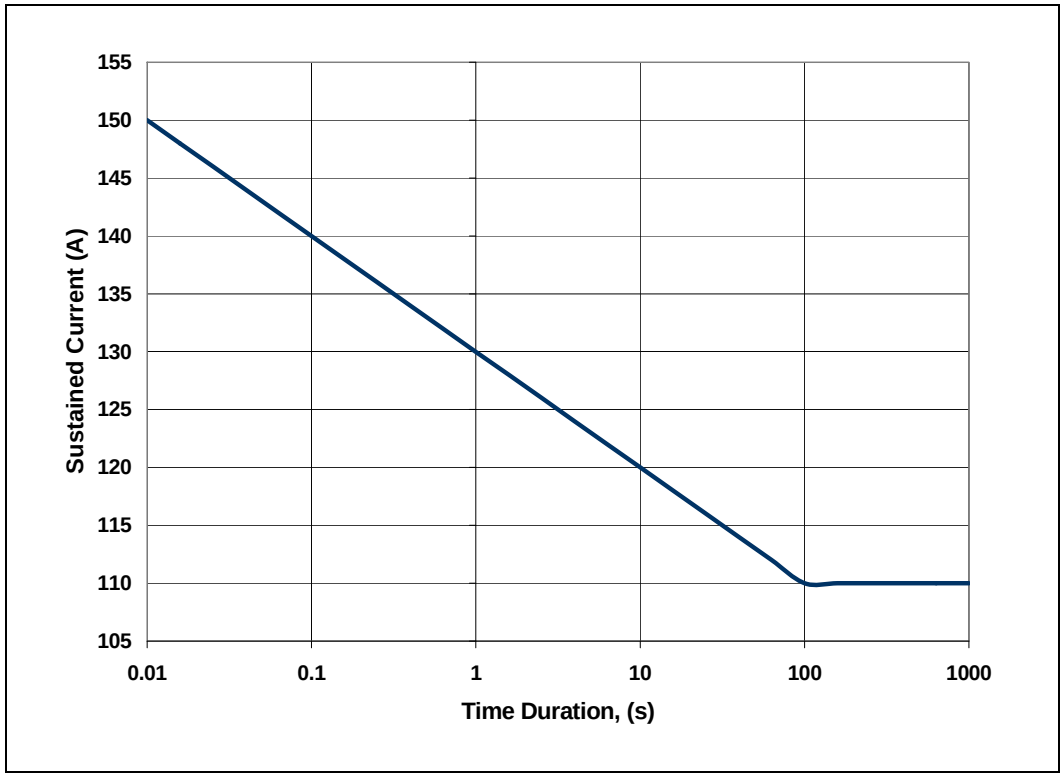


Notes:
1. V_{OS} is the measured overshoot voltage.
2. T_{OS} is the measured time duration above VID.

2.6.2 Die Voltage Validation

Core voltage (V_{CC}) overshoot events at the processor must meet the specifications in Table 2-10 when measured across the VCC_SENSE and VSS_SENSE lands. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

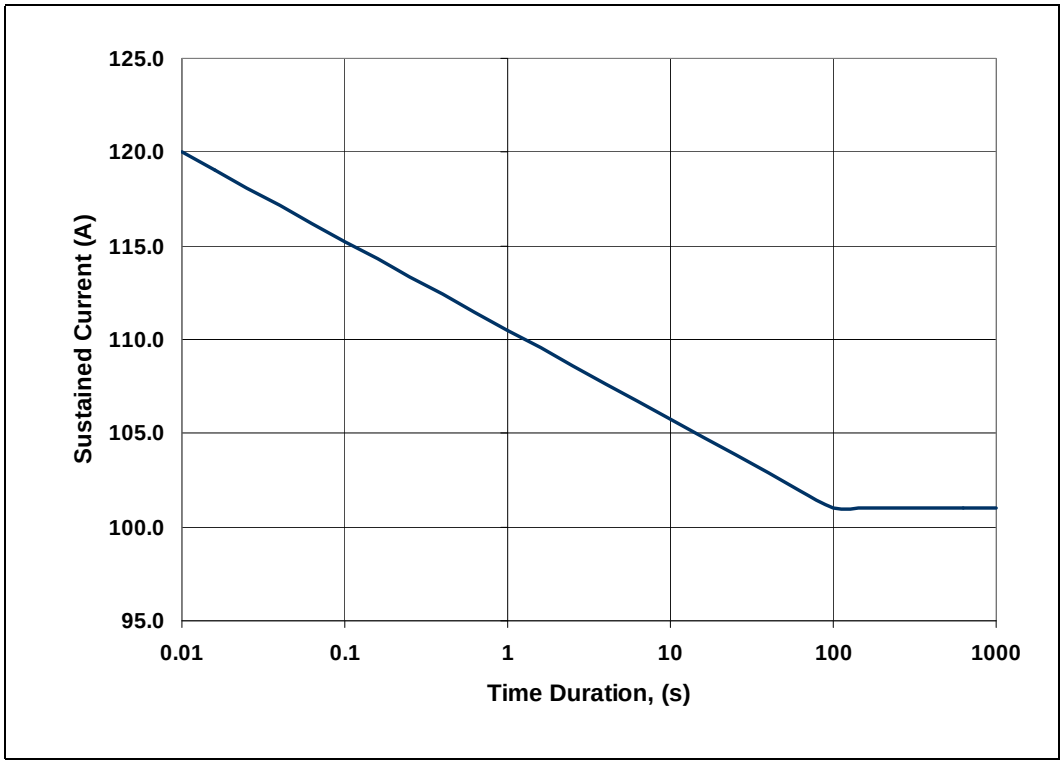
Figure 2-5. Load Current Versus Time (Frequency Optimized Server / Workstation)[1,2]



Notes:

1. Processor or voltage regulator thermal protection circuitry should not trip for load currents greater than I_{CC_TDC}.
2. Not 100% tested. Specified by design characterization.

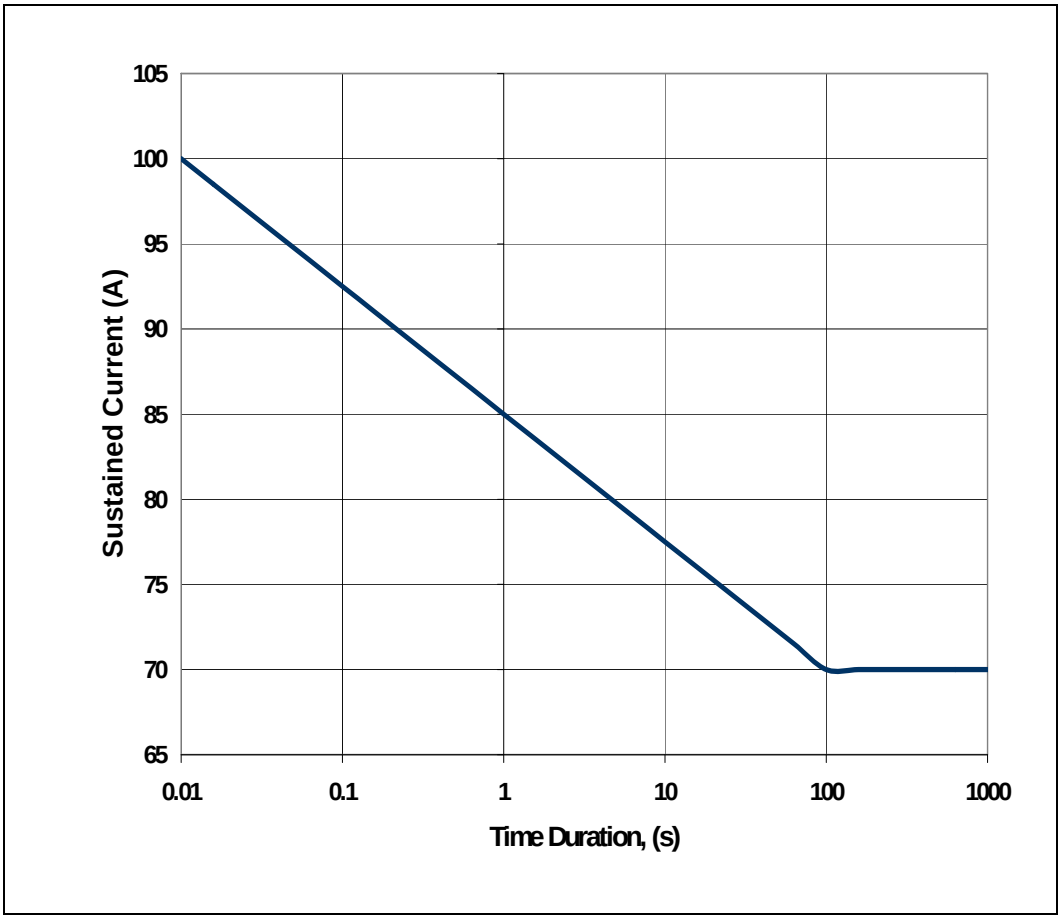
Figure 2-6. Load Current Versus Time (Advanced Server / Workstation)[1,2]



Notes:

1. Processor or voltage regulator thermal protection circuitry should not trip for load currents greater than I_{CC_TDC}.
2. Not 100% tested. Specified by design characterization.

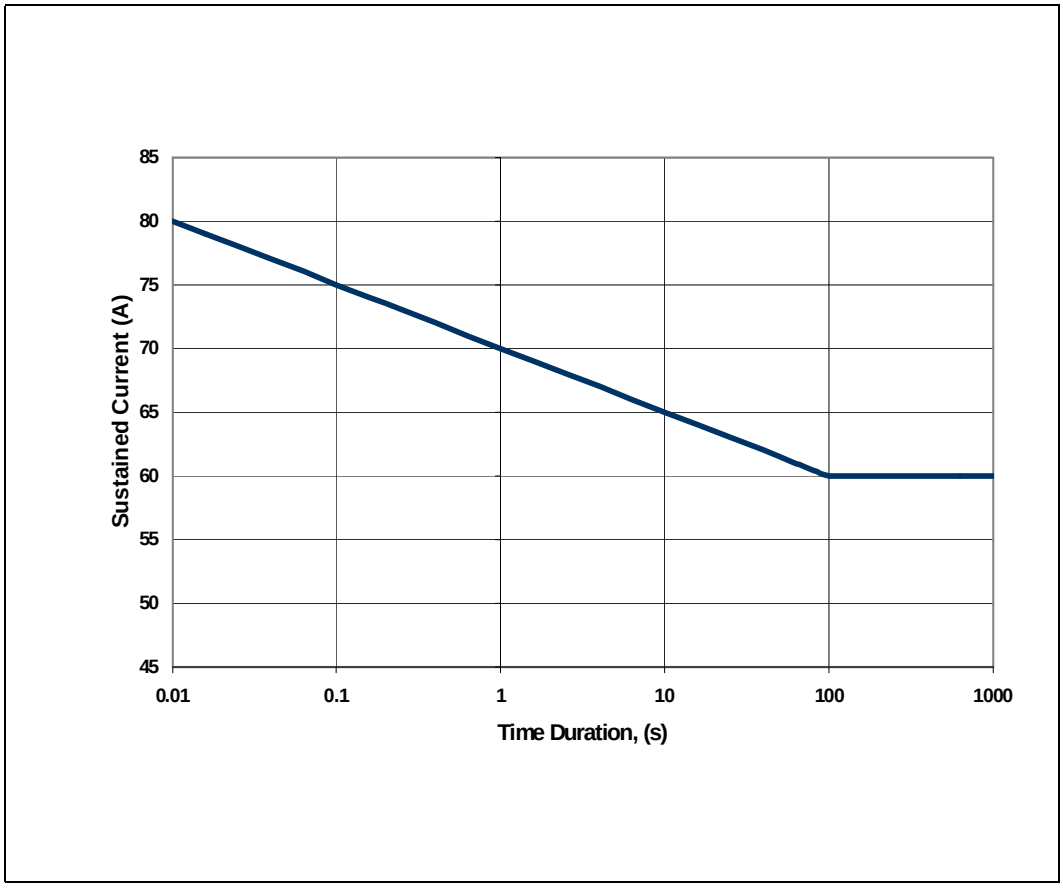
Figure 2-7. Load Current Versus Time (Standard Server / Workstation)[1,2]



Notes:

1. Processor or voltage regulator thermal protection circuitry should not trip for load currents greater than I_{CC_TDC}.
2. Not 100% tested. Specified by design characterization.

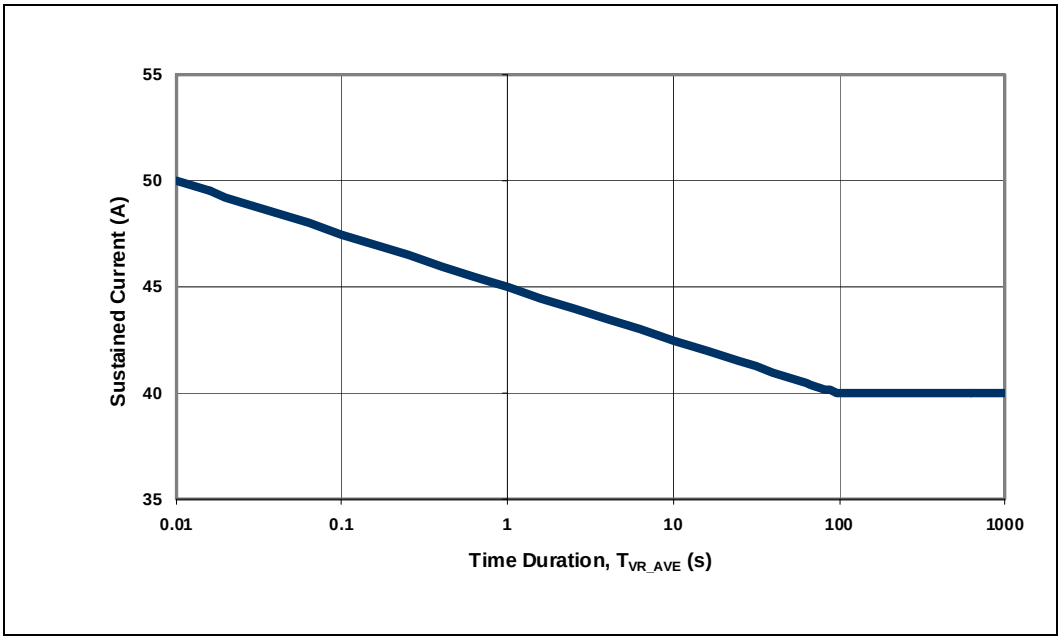
Figure 2-8. Load Current Versus Time (Low Power & LV-60W)[1,2]



Notes:

1. Processor or voltage regulator thermal protection circuitry should not trip for load currents greater than I_{CC_TDC}.
2. Not 100% tested. Specified by design characterization.

Figure 2-9. Load Current Versus Time (Low Power & LV-40W)[1,2]



Notes:

1. Processor or voltage regulator thermal protection circuitry should not trip for load currents greater than I_{CC_TDC}.
2. Not 100% tested. Specified by design characterization.

Table 2-11. V_{TT} Static and Transient Tolerance (Sheet 1 of 2)

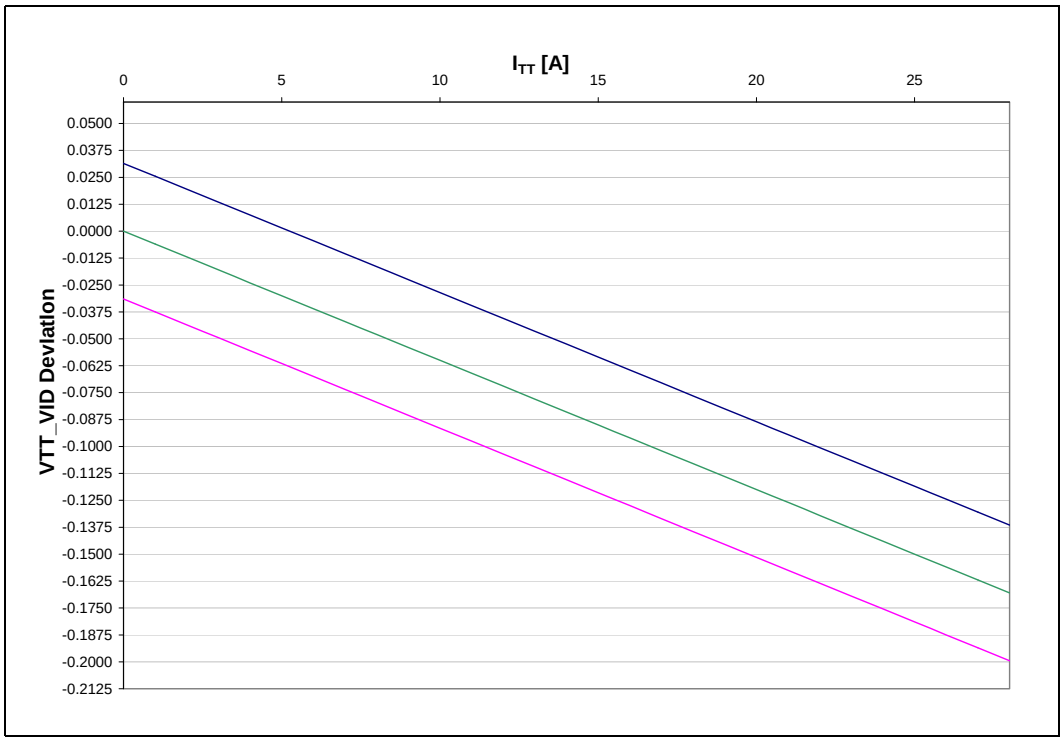
I_{TT} (A)	V_{TT_Max} (V)	V_{TT_Typ} (V)	V_{TT_Min} (V)	Notes[1,2,3,4]
0	VTT_VID + 0.0315	VTT_VID - 0.0000	VTT_VID - 0.0315	
1	VTT_VID + 0.0255	VTT_VID - 0.0060	VTT_VID - 0.0375	
2	VTT_VID + 0.0195	VTT_VID - 0.0120	VTT_VID - 0.0435	
3	VTT_VID + 0.0135	VTT_VID - 0.0180	VTT_VID - 0.0495	
4	VTT_VID + 0.0075	VTT_VID - 0.0240	VTT_VID - 0.0555	
5	VTT_VID + 0.0015	VTT_VID - 0.0300	VTT_VID - 0.0615	
6	VTT_VID - 0.0045	VTT_VID - 0.0360	VTT_VID - 0.0675	
7	VTT_VID - 0.0105	VTT_VID - 0.0420	VTT_VID - 0.0735	
8	VTT_VID - 0.0165	VTT_VID - 0.0480	VTT_VID - 0.0795	
9	VTT_VID - 0.0225	VTT_VID - 0.0540	VTT_VID - 0.0855	
10	VTT_VID - 0.0285	VTT_VID - 0.0600	VTT_VID - 0.0915	
11	VTT_VID - 0.0345	VTT_VID - 0.0660	VTT_VID - 0.0975	
12	VTT_VID - 0.0405	VTT_VID - 0.0720	VTT_VID - 0.1035	
13	VTT_VID - 0.0465	VTT_VID - 0.0780	VTT_VID - 0.1095	
14	VTT_VID - 0.0525	VTT_VID - 0.0840	VTT_VID - 0.1155	
15	VTT_VID - 0.0585	VTT_VID - 0.0900	VTT_VID - 0.1215	
16	VTT_VID - 0.0645	VTT_VID - 0.0960	VTT_VID - 0.1275	
17	VTT_VID - 0.0705	VTT_VID - 0.1020	VTT_VID - 0.1335	
18	VTT_VID - 0.0765	VTT_VID - 0.1080	VTT_VID - 0.1395	

Table 2-11. V_{TT} Static and Transient Tolerance (Sheet 2 of 2)

I_{TT} (A)	V_{TT_Max} (V)	V_{TT_Typ} (V)	V_{TT_Min} (V)	Notes[1,2,3,4]
19	VTT_VID - 0.0825	VTT_VID - 0.1140	VTT_VID - 0.1455	
20	VTT_VID - 0.0885	VTT_VID - 0.1200	VTT_VID - 0.1515	
21	VTT_VID - 0.0945	VTT_VID - 0.1260	VTT_VID - 0.1575	
22	VTT_VID - 0.1005	VTT_VID - 0.1320	VTT_VID - 0.1635	
23	VTT_VID - 0.1065	VTT_VID - 0.1380	VTT_VID - 0.1695	
24	VTT_VID - 0.1125	VTT_VID - 0.1440	VTT_VID - 0.1755	
25	VTT_VID - 0.1185	VTT_VID - 0.1500	VTT_VID - 0.1815	
26	VTT_VID - 0.1245	VTT_VID - 0.1560	VTT_VID - 0.1875	
27	VTT_VID - 0.1305	VTT_VID - 0.1620	VTT_VID - 0.1935	
28	VTT_VID - 0.1365	VTT_VID - 0.1680	VTT_VID - 0.1995	

Note:
1. I_{TT} listed in this table is the sum of I_{TTA} and I_{TTD}.
2. This table is intended to aid in reading discrete points on Figure 2-10.
3. The V_{TT_MIN} and V_{TT_MAX} loadlines represent static and transient limits. Each is characterized by a ±31.5 mV offset from V_{TT_TYP}.
4. The loadlines specify voltage limits at the die measured at the VTTD_SENSE and VSS_SENSE_VTTD lands. Voltage regulation feedback for regulator circuits must also be taken from VTTD_SENSE and VSS_SENSE_VTTD lands.

Figure 2-10. V_{TT} Static and Transient Tolerance Loadlines



Notes:
1. The V_{TT_MIN} and V_{TT_MAX} loadlines represent static and transient limits. Each is characterized by a ±31.5 mV offset from V_{TT_TYP}.
2. Refer to Table 2-4 for processor VTT_VID information.
3. Refer to Table 2-11 for V_{TT} Static and Transient Tolerance.

Table 2-12. DDR3 and DDR3L Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage			0.43*V_{DDQ}	V	2,
V_{IH}	Input High Voltage	0.57*V_{DDQ}			V	3, 4
V_{OL}	Output Low Voltage		(V_{DDQ} / 2)* (R_{ON} /(R_{ON}+R_{VTT_TERM}))		V	6
V_{OH}	Output High Voltage		V_{DDQ} - ((V_{DDQ} / 2)* (R_{ON}/(R_{ON}+R_{VTT_TERM}))		V	4,6
R_{ON}	Clock Buffer On Resistance	21		31	Ω	5
R_{ON}	Command Buffer On Resistance	16		24	Ω	5
R_{ON}	Control Buffer On Resistance	21		31	Ω	5
R_{ON}	Data Buffer On Resistance	21		33	Ω	5
R_{ON}	RESET Buffer On Resistance	5		53	Ω	5
Data ODT	On-Die Termination for Data Signals	45 90		55 110	Ω	7
ParErr ODT	On-Die Termination for Parity Error bits	90		110	Ω	
I_{LI}	Input Leakage Current	N/A	N/A	± 500	mA	
DDR_COMP0	COMP Resistance	99	100	101	Ω	8
DDR_COMP1	COMP Resistance	24.65	24.9	25.15	Ω	8
DDR_COMP2	COMP Resistance	128.7	130	131.3	Ω	8

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{DDQ}. However, input signal drivers must comply with the signal quality specifications. Refer to Section 3.
5. This is the pull down driver resistance.
6. R_{VTT_TERM} is the termination on the DIMM and not controlled by the processor. Please refer to the applicable DIMM datasheet.
7. The minimum and maximum values for these signals are programmable by BIOS to one of the pairs.
8. COMP resistance must be provided on the system board with 1% resistors.

Table 2-13. PECI Signal DC Electrical Limits (Sheet 1 of 2)

Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
V_{In}	Input Voltage Range	-0.150	V_{TTD} + 0.150	V	
$V_{Hysteresis}$	Hysteresis	0.100 * V_{TTD}		V	
V_N	Negative-edge threshold voltage	0.275 * V_{TTD}	0.500 * V_{TTD}	V	2,6
V_P	Positive-edge threshold voltage	0.550 * V_{TTD}	0.725 * V_{TTD}	V	2,6
R_{Pullup}	Pullup Resistance (V_{OH} = 0.75 * V_{TTD})	N/A	50	Ω	
I_{Leak+}	High impedance state leakage to V_{TTD} (V_{leak} = V_{OL})	N/A	50	µA	3

Table 2-13. PECI Signal DC Electrical Limits (Sheet 2 of 2)

Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
I_{Leak-}	High impedance leakage to GND (V_{leak} = V_{OH})	N/A	25	µA	3
C_{Bus}	Bus capacitance per node	N/A	10	pF	4,5
V_{Noise}	Signal noise immunity above 300 MHz	0.100 * V_{TTD}	N/A	V_{p-p}	

Note:
1. V_{TTD} supplies the PECI interface. PECI behavior does not affect V_{TTD} min/max specifications.
2. It is expected that the PECI driver will take into account, the variance in the receiver input thresholds and consequently, be able to drive its output within safe limits (-0.150 V to 0.275*V_{TTD} for the low level and 0.725*V_{TTD} to V_{TTD}+0.150 for the high level).
3. The leakage specification applies to powered devices on the PECI bus.
4. One node is counted for each client and one node for the system host. Extended trace lengths might appear as additional nodes.
5. Excessive capacitive loading on the PECI line may slow down the signal rise/fall times and consequently limit the maximum bit rate at which the interface can operate.
6. Please refer to Figure 2-2 for further information.

Table 2-14. System Reference Clock DC Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes[1]
$V_{BCLK\_diff\_ih}$	Differential Input High Voltage	0.150	N/A	V		
$V_{BCLK\_diff\_il}$	Differential Input Low Voltage	N/A	-0.150	V		
V_{cross} (abs)	Absolute Crossing Point	0.250	0.550	V	2-16 2-19	2, 4
V_{cross}(rel)	Relative Crossing Point	0.250 + 0.5*(VH_{avg} - 0.700)	0.550 + 0.5*(VH_{avg} - 0.700)	V	2-16	3,4,5
ΔV_{cross}	Range of Crossing Points	N/A	0.140	V	2-20	6

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as the instantaneous voltage value when the rising edge of BCLK_DN is equal to the falling edge of BCLK_DP.
3. V_{Havg} is the statistical average of the VH measured by the oscilloscope.
4. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
5. V_{Havg} can be measured directly using “Vtop” on Agilent* and “High” on Tektronix* oscilloscopes.
6. V_{CROSS} is defined as the total variation of all crossing voltages as defined in Note 2.

Table 2-15. RESET# Signal DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage			0.6 * V_{TTA}	V	2
V_{IH}	Input High Voltage	0.7 * V_{TTA}			V	2,4
R_{ON}	Buffer On Resistance	10		18	Ω	
I_{LI}	Input Leakage Current			± 200	µA	3

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{TTA} referred to in these specifications refers to instantaneous V_{TTA}.
3. For V_{IN} between 0 V and V_{TTA}. Measured when the driver is tri-stated.
4. V_{IH} may experience excursions above V_{TT}. However, input signal drivers must comply with the signal quality specifications in Section 3.

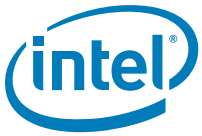


Table 2-16. TAP Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage			0.40 * V_{TTA}	V	2
V_{IH}	Input High Voltage	0.60 * V_{TTA}			V	2,4
V_{OL}	Input Low Voltage			V_{TTA} * R_{ON} / (R_{ON} + R_{sys_term})	V	2
V_{OH}	Input High Voltage	V_{TTA}			V	2,4
R_{ON}	Buffer On Resistance	10		18	Ω	
I_{LI}	Input Leakage Current			± 200	µA	3

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{TTA} referred to in these specifications refers to instantaneous V_{TTA}.
3. For V_{IN} between 0 V and V_{TTA}. Measured when the driver is tri-stated.
4. V_{IH} and V_{OH} may experience excursions above V_{TT}. However, input signal drivers must comply with the signal quality specifications in Section 3.

Table 2-17. xxxPWRGOOD Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage for VCCPWRGOOD and VTTPWRGOOD signals			0.25 * V_{TTA}	V	2,5
V_{IL}	Input Low Voltage for VDDPWRGOOD signal			0.29	V	6
V_{IH}	Input High Voltage for VCCPWRGOOD and VTTPWRGOOD signals	0.75 * V_{TTA}			V	2,4,5
V_{IH}	Input High Voltage for VDDPWRGOOD signal	0.87			V	4,6
R_{ON}	Buffer On Resistance	10		18	Ω	
I_{LI}	Input Leakage Current			± 200	µA	3

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{TTA} referred to in these specifications refers to instantaneous V_{TTA}.
3. For V_{IN} between 0 V and V_{TTA}. Measured when the driver is tri-stated.
4. V_{IH} may experience excursions above V_{TT}. However, input signal drivers must comply with the signal quality specifications in Section 3.
5. This specification applies to the VCCPWRGOOD and VTTPWRGOOD signals.
6. This specification applies to the VDDPWRGOOD signal.

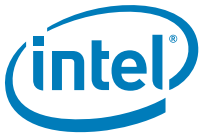
Table 2-18. Processor Sideband Signal Group DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage			0.64 * V_{TTA}	V	2
V_{IL}	Input Low Voltage for PROCHOT# Signal			0.61* V_{TTA}	V	2
V_{IL}	Input Low Voltage for PECI ID Signal			0.15 * V_{TTA}	V	
V_{IH}	Input High Voltage	0.76 * V_{TTA}			V	2
V_{IH}	Input High Voltage for PECI ID Signal	085 * V_{TTA}			V	

Table 2-18. Processor Sideband Signal Group DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{OL}	Output Low Voltage			$V_{TTA} * R_{ON} / (R_{ON} + R_{SYS\_TERM})$	V	2,3
V_{OH}	Output High Voltage	V_{TTA}			V	2
ODT	On-Die Termination	45		55		4
R_{ON}	Buffer On Resistance for Processor Sideband Signals	10		18	Ω	
R_{ON}	Buffer On Resistance for VID[7:0] Signals		100		Ω	
I_{LI}	Input Leakage Current for Processor Sideband Signals			± 200	µA	
I_{LI}	Input Leakage Current for DDR_THERM# and DDR_THERM2# Signals			± 50	µA	5
COMP0	COMP Resistance	49.4	49.9	50.4	Ω	6

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{TTA} referred to in these specifications refers to instantaneous V_{TTA}.
3. R_{SYS_TERM} is the termination on the system and is not controlled by the processor.
4. Applies to all Processor Sideband signals, unless otherwise mentioned in Table 2-6.
5. This specification only applies to DDR_THERM# and DDR_THERM2#signals.
6. COMP resistance must be provided on the system board with 1% resistors. COMP0 resistors are tied to V_{SS}.



2.7 Intel® QuickPath Interconnect Specifications

Intel® QuickPath Interconnect specifications are defined at the processor pins. In most cases, termination resistors are not required as these are integrated into the processor silicon (Refer to Table 2-6).

Table 2-19. Common Intel® QuickPath Interconnect Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Notes
UIavg	Avg UI size at "f" GT/s (f = 4.8, 5.86, or 6.4)	0.999 * Nom	1000/f	1.001 * Nom	psec	
$T_{slew\text{-}rise\text{-}fall\text{-}pin}$	Defined as the slope of the rising or falling waveform as measured between +/- 100 mV of the differential transmitter output, for any data or clock.	10		25	V / nsec	
$Z_{TX\_LOW\_CM\_DC}$	DC resistance of Tx terminations at half the single ended swing (usually $0.25*V_{Tx\text{-}diff\text{-}pp\text{-}pin}$) bias point	38		52	Ω	
$\Delta Z_{TX\_LOW\_CM\_DC}$	Defined as: $\pm(max(Z_{TX\_LOW\_CM\_DC}) - min(Z_{TX\_LOW\_CM\_DC})) / Z_{TX\_LOW\_CM\_DC}$ expressed in %, over full range of Tx single ended voltage	-6	0	6	% of $Z_{TX\_LOW\_CM\_DC}$	
$Z_{RX\_LOW\_CM\_DC}$	DC resistance of Rx terminations at half the single ended swing (usually $0.25*V_{Tx\text{-}diff\text{-}pp\text{-}pin}$) bias point	38		52	Ω	
$\Delta Z_{RX\_LOW\_CM\_DC}$	Defined as: $\pm(max(Z_{RX\_LOW\_CM\_DC}) - min(Z_{RX\_LOW\_CM\_DC})) / Z_{RX\_LOW\_CM\_DC}$ expressed in %, over full range of Rx single ended voltage	-6	0	6	% of $Z_{RX\_LOW\_CM\_DC}$	
$N_{MIN\text{-}UI\text{-}Validation}$	# of UI over which the eye mask voltage and timing spec needs to be validated	1,000,000			UI	
$Z_{TX\_HIGH\_CM\_DC}$	Single ended DC impedance to GND for either D+ or D- of any data bit at Tx	10k			Ω	1
$Z_{RX\_HIGH\_CM\_DC}$	Single ended DC impedance to GND for either D+ or D- of any data bit at Rx	10k			Ω	2
$Z_{TX\_LINK\_DETECT}$	Link Detection Resistor	500		2000	Ω	
$V_{TX\_LINK\_DETECT}$	Link Detection Resistor Pull-up Voltage			1.6	V	
$T_{DATA\_TERM\_SKEW}$	Skew between first to last data termination meeting $Z_{RX\_LOW\_CM\_DC}$			128	UI	
$T_{INBAND\_RESET\_SENSE}$	Time taken by inband reset detector to sense Inband Reset			1.5	µs	
T_{CLK_DET}	Time taken by clock detector to observe clock stability			20k	UI	
$T_{CLK\_FREQ\_DET}$	Time taken by clock frequency detector to decide slow vs. operational clock after stable clock			32	Reference Clock Cycles	
$T_{Refclk\text{-}Tx\text{-}Variability}$	Phase variability between Reference Clk (at Tx input) and Tx output			500	psec	
$T_{Refclk\text{-}jitter\text{-}rms\text{-}onepll}$	Accumulated rms jitter over n UI of a given PLL model output in response to the jittery reference clock input. The PLL output is generated by convolving the measured reference clock phase jitter with a given PLL transfer function. Here n=12.			0.5	psec	
BER_{Lane}	Bit Error Rate per lane valid for 4.8, 5.86 and 6.4 GT/s			1.0E-14	Events	
QPI[1,0]_COMP	COMP Resistance	21.0-1%	21.0	21.0+1%	Ω	

Notes:
1. Used during initialization. It is the state of “OFF” condition for the transmitter. That is, when the output driver is disconnected and only the minimum termination is connected. The link detection resistor is assumed not connected when specifying this parameter.
2. Used during initialization. It is the state of “OFF” condition for the receiver when only the minimum termination is connected.

Table 2-20. Parameter Values for Intel® QuickPath Interconnect Channels at 4.8 GT/s

Symbol	Parameter	Min	Max	Unit	Notes
$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	Transmitter differential swing	800	1400	mV	
$V_{Tx\text{-}cm\text{-}dc\text{-}pin}$	Transmitter output DC common mode, defined as average of V_{D+} and V_{D-}. Use setup of Figure 2-11.	0.23	0.27	Fraction of $V_{TX\text{-}diff\text{-}pp\text{-}pin}$	
$V_{Tx\text{-}cm\text{-}ac\text{-}pin}$	Transmitter output AC common mode, defined as $((V_{D+} + V_{D-})/2 - V_{Tx\text{-}cm\text{-}ac\text{-}pin})$. Use setup of Figure 2-11 and Figure 2-13 for illustration of AC common mode distribution and spec limits.	-0.0375	0.0375	Fraction of $V_{TX\text{-}diff\text{-}pp\text{-}pin}$	
$TX_{duty\text{-}pin}$	Average of UI-UI jitter, using setup of Figure 2-11. This appears as bimodal peaks in UI-UI jitter distribution Figure 2-14.	-0.078	0.078	UI	
$TX_{jitUI\text{-}UI\text{-}1E\text{-}7pin}$	UI-UI jitter measured at Tx output pins with 1E-7 probability, using setup of Figure 2-11. Refer to Figure 2-14 for illustration of UI-UI jitter distribution and spec limits	-0.085	0.085	UI	
$TX_{jitUI\text{-}UI\text{-}1E\text{-}9pin}$	UI-UI jitter measured at Tx output pins with 1E-9 probability, using setup of Figure 2-11. Refer to Figure 2-14 for illustration of UI-UI jitter distribution and spec limits	-0.09	0.09	UI	
$TX_{clk\text{-}acc\text{-}jit\text{-}N\_UI\text{-}1E\text{-}7}$	P-P accumulated jitter out of any Tx data or clock over 0 <= n <= N UI where N=12, measured with 1E-7 probability. Refer to Figure 2-14 for illustration	0	0.15	UI	
$TX_{clk\text{-}acc\text{-}jit\text{-}N\_UI\text{-}1E\text{-}9}$	P-P accumulated jitter out of any Tx data or clock over 0 <= n <= N UI where N=12, measured with 1E-9 probability. Refer to Figure 2-14 for illustration	0	0.17	UI	
$T_{Tx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to the clock lane, as measured at Tx output	-0.4	0.4	UI	
$T_{Rx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to the clock lane, as measured at Tx+ channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.	0	2	UI	1
		-1	1		2
$V_{Rx\text{-}cm\text{-}dc\text{-}pin}$	DC common mode ranges at the Rx input for any data or clock channel, defined as average of V_{D+} and V_{D-}.	145	350	mV	
$V_{Rx\text{-}cm\text{-}ac\text{-}pin}$	AC common mode ranges at the Rx input for any data or clock channel, defined as$((V_{D+} + V_{D-})/2 - V_{RX\text{-}cm\text{-}dc\text{-}pin})$. Refer to Figure 2-13 for illustration.	-50	50	mV	
$T_{Rx\text{-}margin}$	Measured timing margin during receiver margining with any receiver equalizer off or for Tx EQ only based systems	0.1		UI	

Notes:
1. Refers to routing lengths of 10 - 15 inches (25.4 - 38.1 cm).
2. Refers to routing lengths of 0 - 10 inches (0 - 25.4 cm).

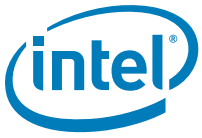


Table 2-21. Parameter Values for Intel® QuickPath Interconnect Channel at 5.86 or 6.4 GT/s

Symbol	Parameter	Min	Max	Unit	Note
$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	Transmitter differential swing	800	1400	mV	
$V_{Tx\text{-}cm\text{-}dc\text{-}pin}$	Transmitter output DC common mode, defined as average of V_{D+} and V_{D-}. Use setup of Figure 2-11.	0.23	0.27	Fraction of $V_{TX\text{-}diff\text{-}pp\text{-}pin}$	
$V_{Tx\text{-}cm\text{-}ac\text{-}pin}$	Transmitter output AC common mode, defined as $((V_{D+} + V_{D-})/2 - V_{TX\text{-}cm\text{-}dc\text{-}pin})$. Use setup of Figure 2-11 and Figure 2-13 for illustration of AC common mode distribution and spec limits.	–0.0375	0.0375	Fraction of $V_{TX\text{-}diff\text{-}pp\text{-}pin}$	
$TX_{duty\text{-}pin}$	Average of UI-UI jitter, using setup of Figure 2-11. This appears as bimodal peaks in UI-UI jitter distribution Figure 2-14	-0.078	0.078	UI	
$TX_{jitUI\text{-}UI\text{-}1E\text{-}7pin}$	UI-UI jitter measured at Tx output pins with 1E-7 probability, using setup of Figure 2-11. Refer to Figure 2-14 for illustration of UI-UI jitter distribution and spec limits	-0.088	0.088	UI	
$TX_{jitUI\text{-}UI\text{-}1E\text{-}9pin}$	UI-UI jitter measured at Tx output pins with 1E-9 probability, using setup of Figure 2-11. Refer to Figure 2-14 for illustration of UI-UI jitter distribution and spec limits.	-0.095	0.095	UI	
$TX_{clk\text{-}acc\text{-}jit\text{-}N\_UI\text{-}1E\text{-}7}$	P-P accumulated jitter out of any Tx data or clock over 0 <= n <= N UI where N=12, measured with 1E-7 probability. Refer to Figure 2-14 for illustration	0	0.15	UI	
$TX_{clk\text{-}acc\text{-}jit\text{-}N\_UI\text{-}1E\text{-}9}$	P-P accumulated jitter out of any Tx data or clock over 0 <= n <= N UI where N=12, measured with 1E-9 probability. Refer to Figure 2-14 for illustration	0	0.17	UI	
$T_{Tx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to clock lane, as measured at Tx output	-0.4	0.4	UI	
$T_{Rx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to the clock lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.	0	2	UI	1
		-1	1		2
$V_{Rx\text{-}cm\text{-}dc\text{-}pin}$	DC common mode ranges at the Rx input for any data or clock channel, defined as average of V_{D+} and V_{D-}.	145	350	mV	
$V_{Rx\text{-}cm\text{-}ac\text{-}pin}$	AC common mode ranges at the Rx input for any data or clock channel, defined as $((V_{D+} + V_{D-})/2 - V_{RX\text{-}cm\text{-}dc\text{-}pin})$. Refer to Figure 2-13 for illustration.	–50	50	mV	
$T_{Rx\text{-}margin}$	Measured timing margin during receiver margining with any receiver equalizer off or forTx EQ only based systems	0.1		UI	
$V_{Rx\text{-}margin}$	Measured voltage margin during receiver margining with receiver equalizer off	40		mV	

Notes:
1. Refers to routing lengths of 10 - 15 inches (25.4 - 38.1 cm).
2. Refers to routing lengths of 0 - 10 inches (0 - 25.4 cm).

2.8 AC Specifications

AC specifications are defined at the processor pads, unless otherwise noted. Therefore, proper simulation is the only means to verify proper timing and signal quality. Care should be taken to read all notes associated with each parameter.

Table 2-22. System Reference Clock AC Specifications (Sheet 1 of 2)

Parameter	Min	Nom	Max	Unit	Figure	Notes[1]
BCLK Frequency (SSC-off)	133.29	133.33	133.37	MHz	2-17	2
BCLK Frequency (SSC-on)	132.62	133.33	133.37	MHz	2-17	2

Table 2-22. System Reference Clock AC Specifications (Sheet 2 of 2)

Parameter	Min	Nom	Max	Unit	Figure	Notes[1]
$ER_{BCLK-diffRise}$, $ER_{BCLK-diffFall}$	1.0		4.0	V/ns	2-18	3
$T_{BCLK-Dutycycle}$	40	50	60	%	2-17	
$T_{BCLK-diff-jit}$			500	ps		4

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. SSC is Spread Spectrum Clocking. The processor core clock frequency is derived from BCLK. The system reference clock to processor core clock ratio is determined during initialization as described in Section 2.1.5.
3. Rise and fall time slopes (V/ns) are measured between +150 mV and -150 mV of the differential output of reference clock.
4. Phase drift between reference clocks at two connected ports.

Table 2-23. DDR3/DDR3L Electrical Characteristics and AC Specifications at 800 MT/s (Sheet 1 of 2)

Symbol	Parameter	Channel 0 Channel 1 Channel 2		Unit	Figure	Note
		Max	Min			
Latency Timings						
tCL – tRCD – tRP	CAS Latency – RAS to CAS Delay – Pre-charge Command Period	6 – 6 – 6		t_{CK}		
Electrical Characteristics						
T_{SLR_D}	DQ[63:0], DQS_N[17:0], DQS_P[17:0], ECC[7:0] Input Slew Rate	4.0	1.0	V/ns		2
Clock Timings						
T_{CK}	CLK Period	3	2.50	ns		
T_{CH}	CLK High Time	1.50	1.25	ns		
T_{CL}	CLK Low Time	1.50	1.25	ns		
T_{SKEW}	Skew Between Any System Memory Differential Clock Pair (CLK_P/CLK_N)		+155	ps		
Command Signal Timings						
T_{CMD_CO}	RAS#, CAS#, WE#, MA[15:0], BA[2:0] Edge placement accuracy	+375	-375	ps	2-22	3,4,6
Control Signal Timings						
T_{CTRL_CS}	CS#[7:0], CKE[3:0], ODT[3:0] Edge placement accuracy	+375	-375	ps	2-22	3,6
Data and Strobe Signal Timings						
$T_{DVA} + T_{DVB}$	DQ[63:0] Valid before and after DQS[17:0] Rising or Falling Edge		0.67 * UI	UI		7
$T_{SU} + T_{HD}$	DQ Input Setup plus Hold Time to DQS Rising or Falling Edge		0.25 * UI	ns	2-23	1,2,7
T_{DQS_CO}	DQS Edge Placement Accuracy to CK Rising Edge BEFORE write leveling	+375	-375	ns		3,6,7

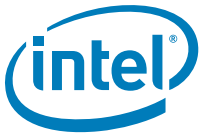


Table 2-23. DDR3/DDR3L Electrical Characteristics and AC Specifications at 800 MT/s (Sheet 2 of 2)

Symbol	Parameter	Channel 0 Channel 1 Channel 2		Unit	Figure	Note
		Max	Min			
T_{DQS_CO}	DQS Edge Placement Accuracy to CK Rising Edge AFTER write leveling	+275	-275	ns		3,6,7,8
T_{WPRE}	DQS/DQS# Write Preamble Duration		2.379	ns		
T_{WPST}	DQS/DQS# Write Postamble Duration	1.371	1.129	ns		
T_{DQSS}	CK Rising Edge Output Access Time, Where a Write Command Is Referenced, to the First DQS Rising Edge	C_{WL} x (T_{CK} + 4)		ns		5,6

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. Timing specifications only depend on the operating frequency of the memory channel and not the maximum rated frequency.
2. When the single ended slew rate of the input Data or Strobe signals, within a byte group, are below 1.0 V/ns, the tSU and tHD specifications must be increased by a derating factor. The input single ended slew rate is measured DC to AC levels; V_{IL}_DC to V_{IH}_AC for rising edges, and V_{IH}_DC to V_{IL}_AC for falling edges. Use the worse case minimum slew rate measured between Data and Strobe, within a byte group, to determine the required derating value. No derating is required for single ended slew rates equal to or greater than 1.0 V/ns.
3. Edge Placement Accuracy (EPA): The silicon contains digital logic that automatically adjusts the timing relationship between the DDR reference clocks and DDR signals. The BIOS initiates a training procedure that will place a given signal appropriately within the clock period. The difference in delay between the signal and clock is accurate to within +/- EPA. This EPA includes jitter, skew, within die variation and several other effects.
4. Data to Strobe read setup and Data from Strobe read hold minimum requirements specified at the processor pad are determined with the minimum Read DQS/DQS# delay.
5. C_{WL} (CAS Write Latency) is the delay, in clock cycles, between the rising edge of CK where a write command is referenced and the first rising strobe edge where the first byte of write data is present. The C_{WL} value is determined by the value of the CL (CAS Latency) setting.
6. The system memory clock outputs are differential (CLK and CLK#), the CLK rising edge is referenced at the crossing point where CLK is rising and CLK# is falling.
7. The system memory strobe outputs are differential (DQS and DQS#), the DQS rising edge is referenced at the crossing point where DQS is rising and DQS# is falling, and the DQS falling edge is referenced at the crossing point where DQS is falling and DQS# is rising.
8. This values specifies the parameter after write leveling, representing the residual error in the controller after training, and does not include any effects from the DRAM itself.

Table 2-24. DDR3 Electrical Characteristics and AC Specifications at 1066 MT/s (Sheet 1 of 2)

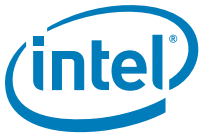
Symbol	Parameter	Channel 0 Channel 1 Channel 2		Unit	Figure	Note
		Max	Min			
Latency Timings						
tCL – tRCD – tRP	CAS Latency – RAS to CAS Delay – Pre-charge Command Period	7 – 7 – 7 8 - 8 - 8		tCK		
Electrical Characteristics						
T_{SLR_D}	DQ[63:0], DQS_P[17:0], DQS_N[17:0], ECC[7:0] Input Slew Rate	4.0	1.0	V/ns		2

Table 2-24. DDR3 Electrical Characteristics and AC Specifications at 1066 MT/s (Sheet 2 of 2)

Symbol	Parameter	Channel 0 Channel 1 Channel 2		Unit	Figure	Note
		Max	Min			
Clock Timings						
T_{CK}	CLK Period	<2.50	1.875	ns		
T_{CH}	CLK High Time	1.25	0.94	ns		
T_{CL}	CLK Low Time	1.25	0.94	ns		
T_{SKEW}	Skew Between Any System Memory Differential Clock Pair (CLK_P/CLK_N)		+155	ps		
Command Signal Timings						
T_{CMD_CO}	RAS#, CAS#, WE#, MA[15:0], BA[2:0] Edge placement accuracy	+300	-300	ps	2-22	3,4,6
Control Signal Timings						
T_{CTRL_CS}	CS#[7:0], CKE[3:0], ODT[3:0] Edge placement accuracy	+300	-300	ps	2-22	3,6
Data and Strobe Signal Timings						
$T_{DVA} + T_{DVB}$	DQ[63:0] Valid before and after DQS[17:0] Rising or Falling Edge		0.67 * UI	UI		7
$T_{SU} + T_{HD}$	DQ Input Setup plus Hold Time to DQS Rising or Falling Edge		0.25 * UI	ns	2-23	1,2,7
T_{DQS_CO}	DQS Edge Placement Accuracy to CK Rising Edge BEFORE write leveling	+300	-300	ns		3,6,7
T_{DQS_CO}	DQS Edge Placement Accuracy to CK Rising Edge AFTER write leveling	+206	-206	ns		3,6,7,8
T_{WPRE}	DQS/DQS# Write Preamble Duration		1.781	ns		
T_{WPST}	DQS/DQS# Write Postamble Duration	1.031	0.844	ns		
T_{DQSS}	CK Rising Edge Output Access Time, Where a Write Command Is Referenced, to the First DQS Rising Edge	C_{WL} x (T_{CK} + 4)		ns		5,6

Notes:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. When the single ended slew rate of the input Data or Strobe signals, within a byte group, are below 1.0 V/ns, the tSU and tHD specifications must be increased by a derating factor. The input single ended slew rate is measured DC to AC levels; V_{IL}_DC to V_{IH}_AC for rising edges, and V_{IH}_DC to V_{IL}_AC for falling edges. Use the worse case minimum slew rate measured between Data and Strobe, within a byte group, to determine the required derating value. No derating is required for single ended slew rates equal to or greater than 1.0 V/ns.
3. Edge Placement Accuracy (EPA): The silicon contains digital logic that automatically adjusts the timing relationship between the DDR reference clocks and DDR signals. The BIOS initiates a training procedure that will place a given signal appropriately within the clock period. The difference in delay between the signal and clock is accurate to within +/- EPA. This EPA includes jitter, skew, within die variation and several other effects.
4. Data to Strobe read setup and Data from Strobe read hold minimum requirements specified at the processor pad are determined with the minimum Read DQS/DQS# delay.
5. CWL (CAS Write Latency) is the delay, in clock cycles, between the rising edge of CK where a write command is referenced and the first rising strobe edge where the first byte of write data is present. The CWL value is determined by the value of the CL (CAS Latency) setting.



6. The system memory clock outputs are differential (CLK and CLK#), the CLK rising edge is referenced at the crossing point where CLK is rising and CLK# is falling.
7. The system memory strobe outputs are differential (DQS and DQS#), the DQS rising edge is referenced at the crossing point where DQS is rising and DQS# is falling, and the DQS falling edge is referenced at the crossing point where DQS is falling and DQS# is rising.
8. This values specifies the parameter after write leveling, representing the residual error in the controller afrter training, and does not include any effects from the DRAM itself.

Table 2-25. DDR3/DDR3L Electrical Characteristics and AC Specifications at 1333 MT/s (Sheet 1 of 2)

Symbol	Parameter	Channel 0 Channel 1 Channel 2		Unit	Figure	Note
		Max	Min			
System Memory Latency Timings						
tCL – tRCD – tRP	CAS Latency – RAS to CAS Delay – Pre-charge Command Period	8 - 8 - 8 9 - 9 - 9		tCK		
Electrical Characteristics						
T_{SLR_D}	DQ[63:0], DQS_N[17:0], DQS_P[17:0], ECC[7:0], MA[15:0] Input Slew Rate	4.0	1.0	V/ns		2
System Memory Clock Timings						
T_{CK}	CLK Period	<1.875	1.50	ns		
T_{CH}	CLK High Time	0.94	0.75	ns		
T_{CL}	CLK Low Time	0.94	0.75	ns		
T_{SKEW}	Skew Between Any System Memory Differential Clock Pair (CLK_P/CLK_N)		+155	ps		
System Memory Command Signal Timings						
T_{CMD_CO}	RAS#, CAS#, WE#, MA[15:0], BA[2:0] Edge placement accuracy	+250	-250	ps	2-22	3,4,6
System Memory Control Signal Timings						
T_{CTRL_CS}	CS#[7:0], CKE[3:0], ODT[3:0] Edge placement accuracy	+250	-250	ps	2-22	3,6
System Memory Data and Strobe Signal Timings						
$T_{DVA} + T_{DVB}$	DQ[63:0] Valid before and after DQS[17:0] Rising or Falling Edge		0.67 * UI	UI		7
$T_{SU} + T_{HD}$	DQ Input Setup plus Hold Time to DQS Rising or Falling Edge		0.25 * UI	ns		1,2,7
T_{DQS_CO}	DQS Edge Placement Accuracy to CK Rising Edge BEFORE write leveling	+250	-250	ns	2-24	3,6,7
T_{DQS_CO}	DQS Edge Placement Accuracy to CK Rising Edge AFTER write leveling	+165	-165	ns	2-24	3,6,7,8

Table 2-25. DDR3/DDR3L Electrical Characteristics and AC Specifications at 1333 MT/s (Sheet 2 of 2)

Symbol	Parameter	Channel 0 Channel 1 Channel 2		Unit	Figure	Note
		Max	Min			
T_{WPRE}	DQS/DQS# Write Preamble Duration		1.425	ns		
T_{WPST}	DQS/DQS# Write Postamble Duration	0.825	0.674	ns		
T_{DQSS}	CK Rising Edge Output Access Time, Where a Write Command Is Referenced, to the First DQS Rising Edge	C_{WL} x (T_{CK} + 4)		ns		5,6

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. When the single ended slew rate of the input Data or Strobe signals, within a byte group, are below 1.0 V/ns, the tSU and tHD specifications must be increased by a derating factor. The input single ended slew rate is measured DC to AC levels; V_{IL}_DC to V_{IH}_AC for rising edges, and V_{IH}_DC to V_{IL}_AC for falling edges. Use the worse case minimum slew rate measured between Data and Strobe, within a byte group, to determine the required derating value. No derating is required for single ended slew rates equal to or greater than 1.0 V/ns.
3. Edge Placement Accuracy (EPA): The silicon contains digital logic that automatically adjusts the timing relationship between the DDR reference clocks and DDR signals. The BIOS initiates a training procedure that will place a given signal appropriately within the clock period. The difference in delay between the signal and clock is accurate to within +/- EPA. This EPA includes jitter, skew, within die variation and several other effects.
4. Data to Strobe read setup and Data from Strobe read hold minimum requirements specified at the processor pad are determined with the minimum Read DQS/DQS# delay.
5. CWL (CAS Write Latency) is the delay, in clock cycles, between the rising edge of CK where a write command is referenced and the first rising strobe edge where the first byte of write data is present. The CWL value is determined by the value of the CL (CAS Latency) setting.
6. The system memory clock outputs are differential (CLK and CLK#), the CLK rising edge is referenced at the crossing point where CLK is rising and CLK# is falling.
7. The system memory strobe outputs are differential (DQS and DQS#), the DQS rising edge is referenced at the crossing point where DQS is rising and DQS# is falling, and the DQS falling edge is referenced at the crossing point where DQS is falling and DQS# is rising.
8. This values specifies the parameter after write leveling, representing the residual error in the controller afrter training, and does not include any effects from the DRAM itself.

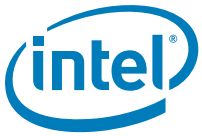


Table 2-26. Processor Sideband Signal Group AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes 1,2,3,4
Asynchronous GTL input pulse width	8		BCLKs		
Tb: V_{TT} stable to VTTPWRGOOD assertion	1	500	ms	2-28	5,7,8,10
Td: VTTPWRGOOD assertion to Dynamic V_{TT} VID from Processor		10	µs	2-28	9
Te: V_{DDQ} stable to VDDPWRGOOD assertion	100		ns	2-28	5,6,7
Tf: VTTPWRGOOD to valid VID	0	10	µs	2-28	
Th: V_{CC} stable to VCCPWRGOOD assertion	0.05	650	ms	2-28	
Ti: V_{CCPLL} stable to VCCPWRGOOD assertion	1		ms	2-28	
Tj: BCLK stable to VCCPWRGOOD assertion	10		BCLKs	2-28	
Tk: VCCPWRGOOD assertion to RESET# de-assertion	1	10	ms	2-28	
Tm: VTTPWRGOOD assertion to VCCPWRGOOD assertion	1		ms	2-28	
Tn: V_{CCPLL} rise time		1.5	ms	2-28	14
Tq: PROCHOT# pulse width	500		µs	2-26	
Tr:THERMTRIP# assertion until V_{CC} / V_{TT} removed		500	ms	2-27	
VTTPWRGOOD de-assertion to V_{TT} below specification	100		ns		
T_{CO}: Time from BCLK land until signal valid at output	0.5	2.275	ns		11
T_{SU}: Processor Sideband Input signals with respect to BCLK	600		ps		12
T_H: Processor Sideband Input signals with respect to BCLK	600		ps		
T_H: Power-On Configuration Hold Time (PROCHOT#)	106		BCLK	8-1	13

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All AC timings for the Asynchronous GTL signals are referenced to the BCLK_P rising edge at Crossing Voltage (V_{CROSS}). VCCPWRGOOD, VTTPWRGOOD and VDDPWRGOOD are referenced to BCLK_P rising edge at 0.5 * V_{TT}.
3. These signals may be driven asynchronously.
4. Refer to Section 8 for additional timing requirements for entering and leaving low power states.
5. xxPWRGOOD signal has no edge rate requirement, but edge must be monotonic.
6. VDDPWRGOOD must be asserted no later then VCCPWRGOOD. There is no releationship between VDDPWRGOOD and VCC ramp.
7. There is no dependency between VDDPWRGOOD and VTTPWRGOOD assertion.
8. VTTPWRGOOD must accurately reflect the state of VTT and must not glitch whenever VTT or VDD is applied.
9. VTT must read VTTFINAL before VCCPWRGOOD assertion.
10. It may be required to add delay on the board to meet the 1 ms minimum processor requirement.
11. Based on a test load of 50 Ω to V_{TT}.
12. Specified for synchronous signals.
13. Applies to PROCHOT# signal only. Please see Section 2.1.7.3.1 and Section 8.1 for information regarding Power-On Configuration options.
14. Rise time is measured from 10% to 90% of the final voltage.

Table 2-27. TAP Signal Group AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes 1,2,3
TCK Period	31.25		ns		
T_s: TDI, TMS Setup Time	1		ns	2-25	
T_h: TDI, TMS Hold Time	1		ns	2-25	
T_x: TDO Clock to Output Delay	0.5	4	ns	2-25	
T_q: TRST# Assert Time	2		T_{TCK}	2-26	

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. It is recommended that TMS be asserted while TRST# is being deasserted.

Table 2-28. VID Signal Group AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes[1]
Ta: VID Step Time	1.25		µs	2-29	
Tb: VID Down Transition to Valid V_{CC} (min)		0	µs	2-29	
Tc: VID Up Transition to Valid V_{CC} (min)		15	µs	2-29	
Td: VID Down Transition to Valid V_{CC} (max)		15	µs	2-29	
Te: VID Up Transition to Valid V_{CC} (max)		0	µs	2-29	

Notes:
1. Platform support for VID transitions is required for the processor to operate within specifications.

2.9 Processor AC Timing Waveforms

The following figures are to be used in conjunction with the AC specifications included in Table 2-19 through Table 2-28.

Note: For Figure 2-11 through Figure 2-29, the following apply:

1. All System Reference Clock signal AC specifications are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK_DP and BCLK_DN at rising edge of BCLK_DP.
2. All TAP signal group AC specifications are referenced to the TCK at 0.5 * V_{TT} at the processor lands. All TAP signal group timings (TMS, TDI, and so forth) are referenced at 0.5 * V_{TT} at the processor die (pads).
3. All CMOS signal AC specifications are referenced at 0.5 * V_{TT} at the processor lands.

The Intel QuickPath Interconnect electrical test setup are shown in Figure 2-11 and Figure 2-12.

Figure 2-11. Intel® QuickPath Interconnect Electrical Test Setup for Validating Standalone TX Voltage and Timing Parameters

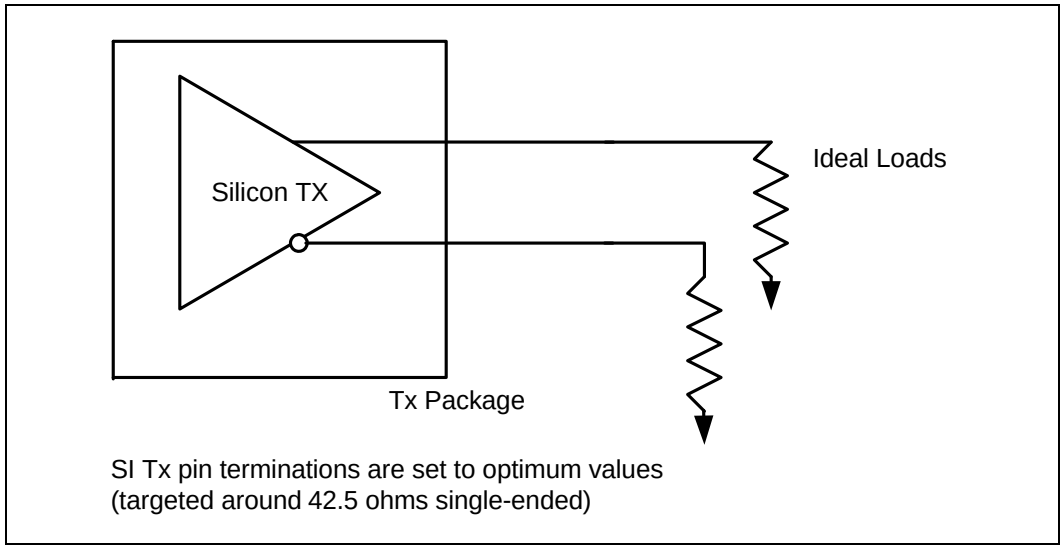


Figure 2-12. Intel® QuickPath Interconnect Electrical Test Setup for Validating TX + Worst-Case Interconnect Specifications

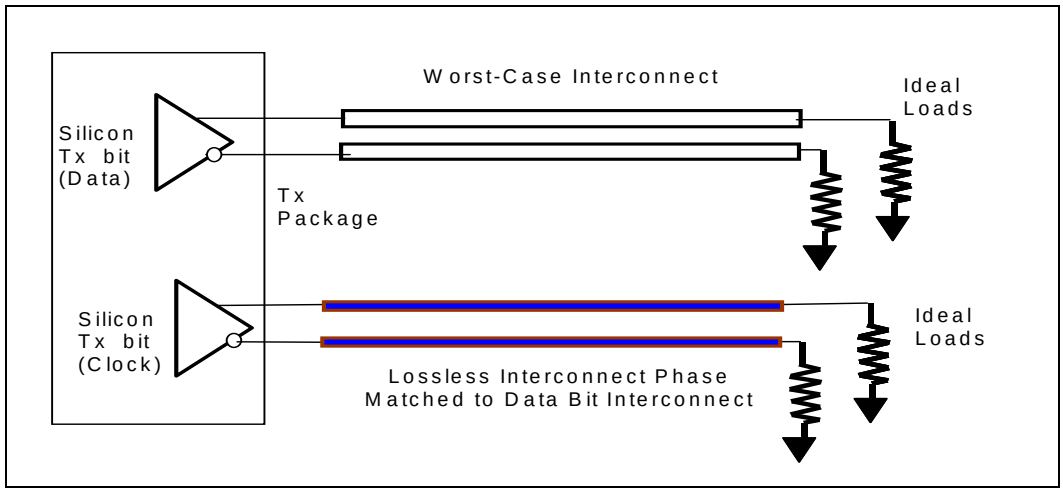


Figure 2-13. Distribution Profile of Common Mode Noise for Either Tx or Rx

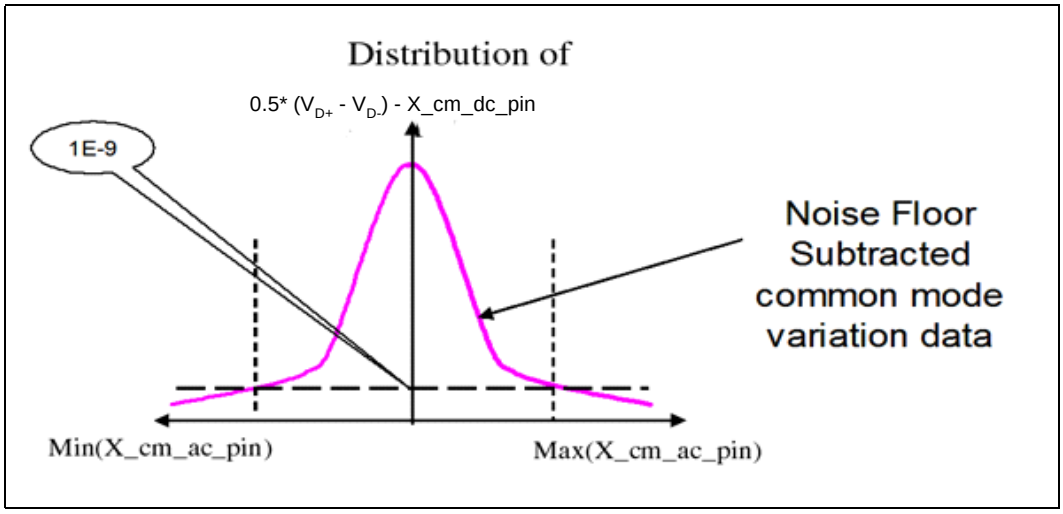


Figure 2-14. Distribution Profile of UI-UI Jitter and Accumulated Jitter

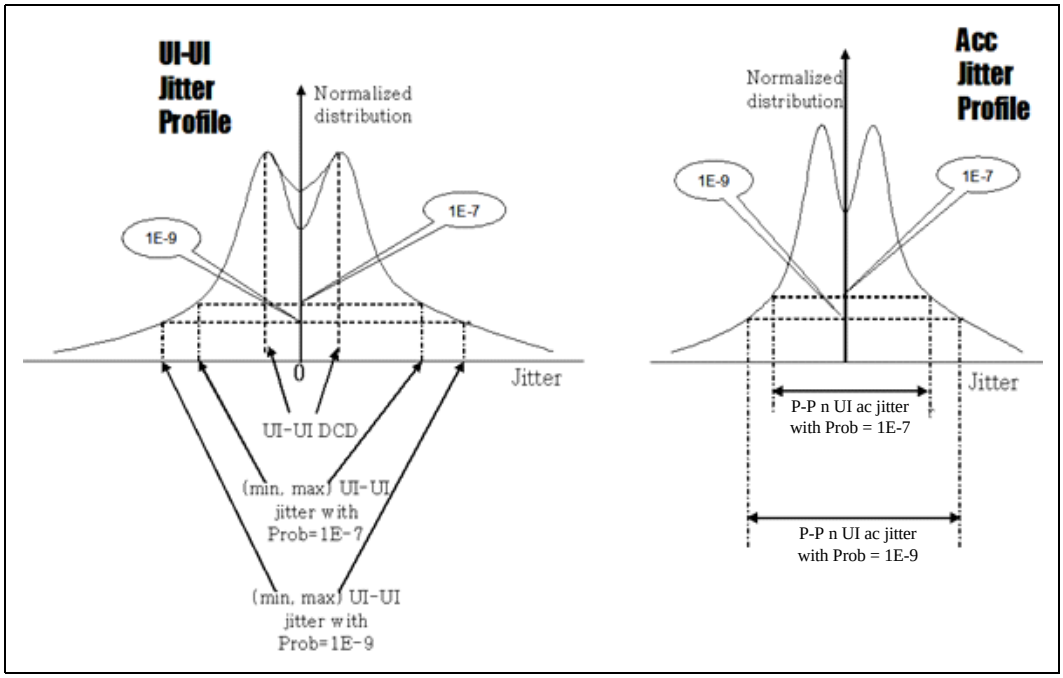


Figure 2-15. Eye Mask at the End of Tx + Channel

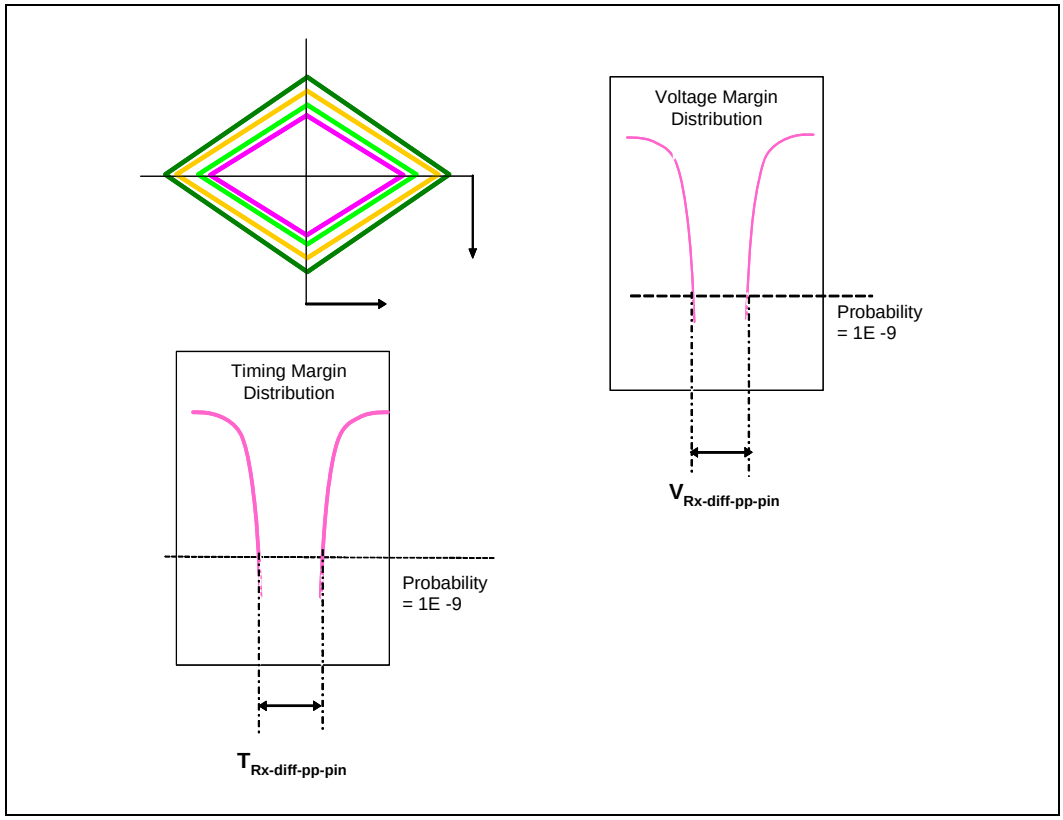


Figure 2-16. Differential Clock Crosspoint Specification

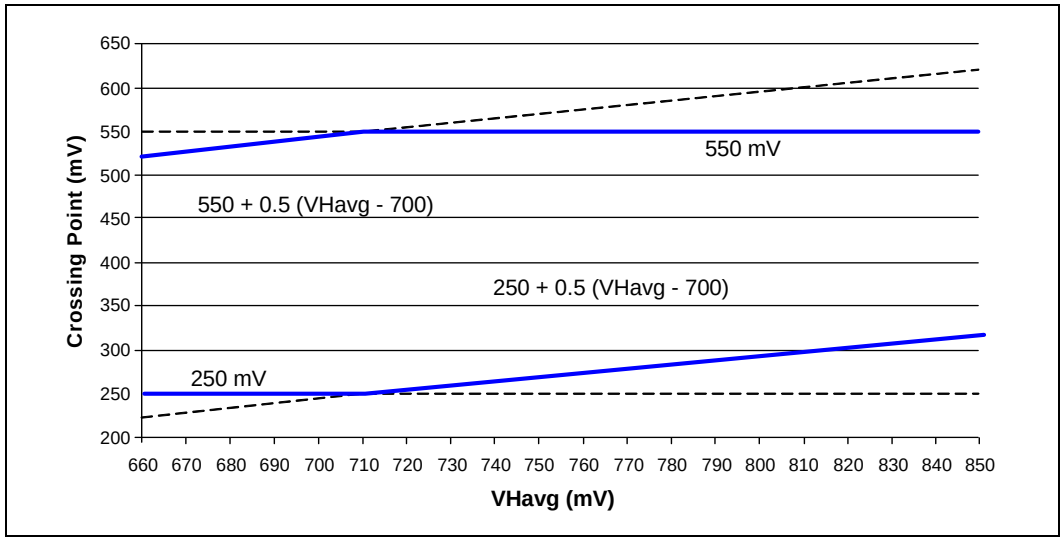


Figure 2-17. Differential Clock Measurement Points for Duty Cycle and Period

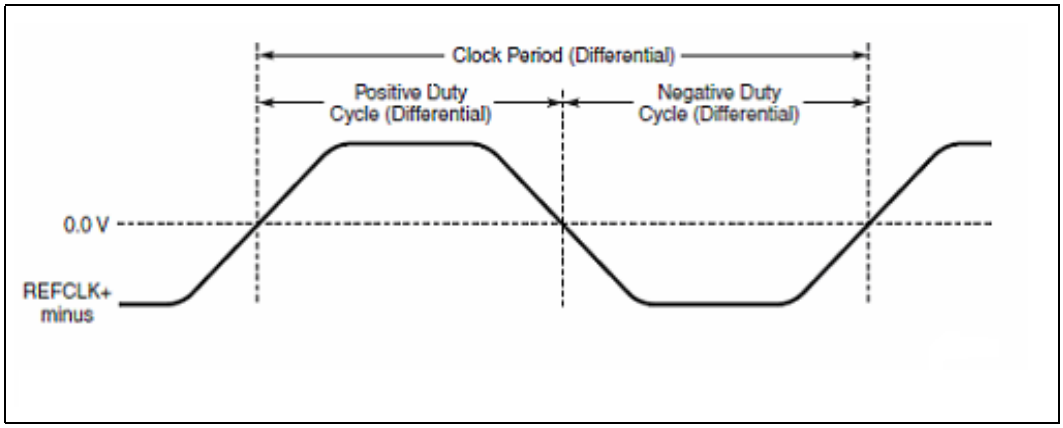


Figure 2-18. Differential Clock Measurement Points for Rise and Fall time

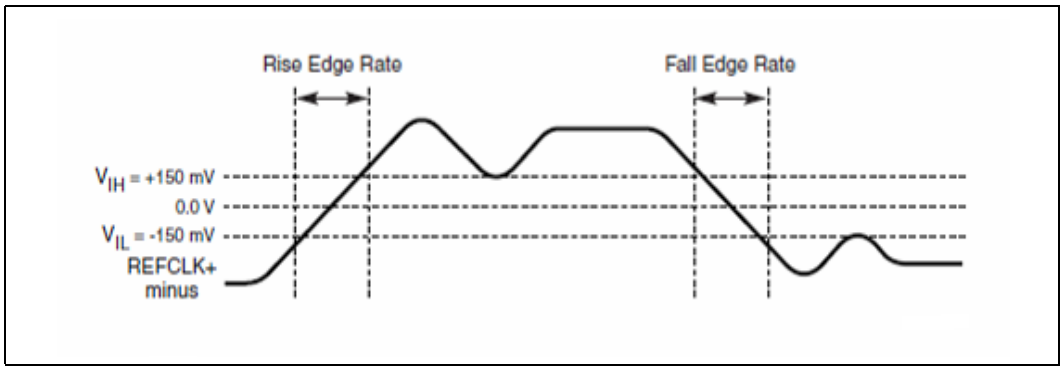


Figure 2-19. Single-Ended Clock Measurement Points for Absolute Cross Point and Swing

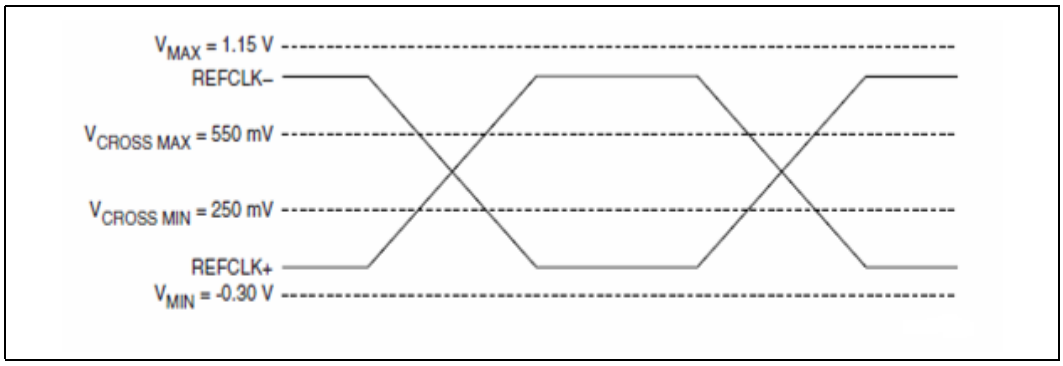


Figure 2-20. Single-Ended Clock Measurement Points for Delta Cross Point

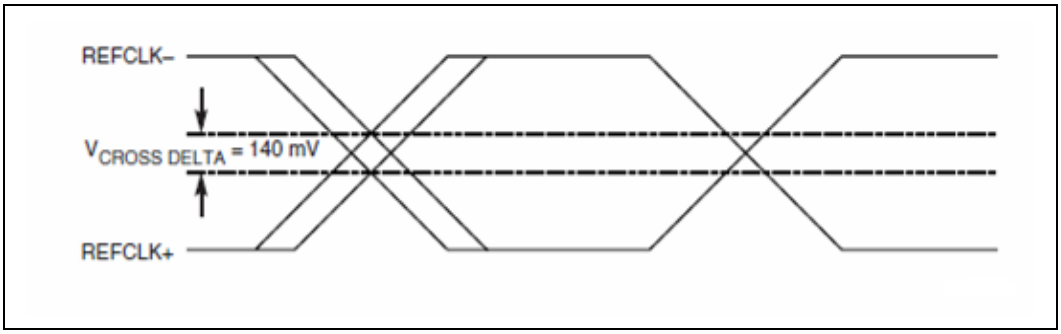


Figure 2-21. Differential Clock Measurement Point for Ringback

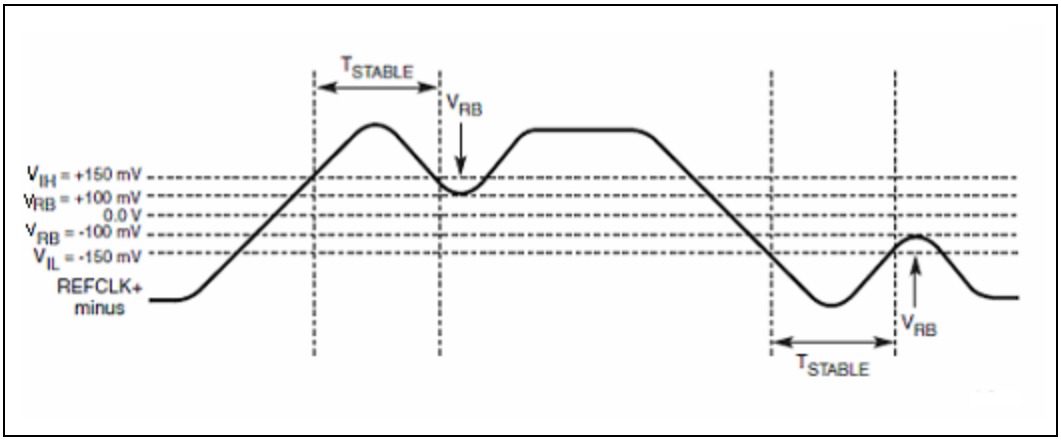


Figure 2-22. DDR3 Command / Control and Clock Timing Waveform

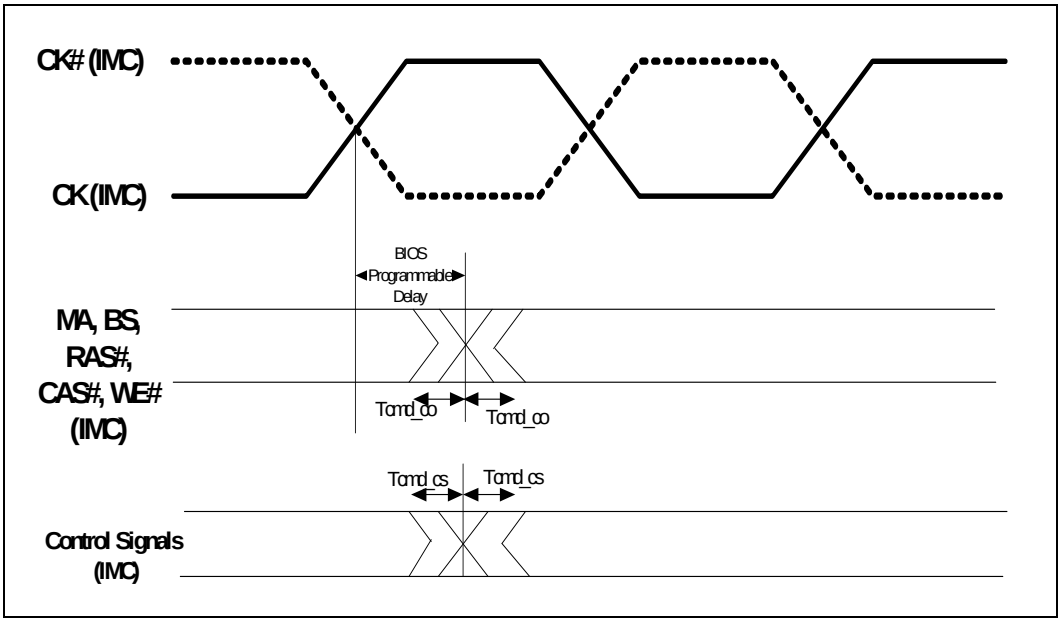


Figure 2-23. DDR3 Clock to Output Timing Waveform

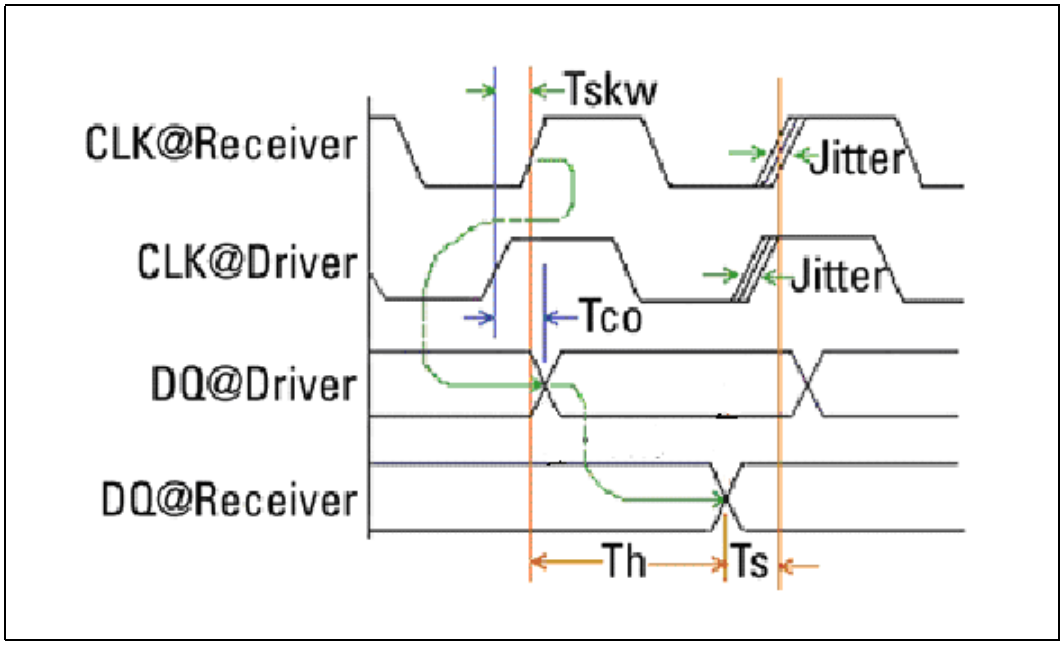


Figure 2-24. DDR3 Clock to DQS Skew Timing Waveform

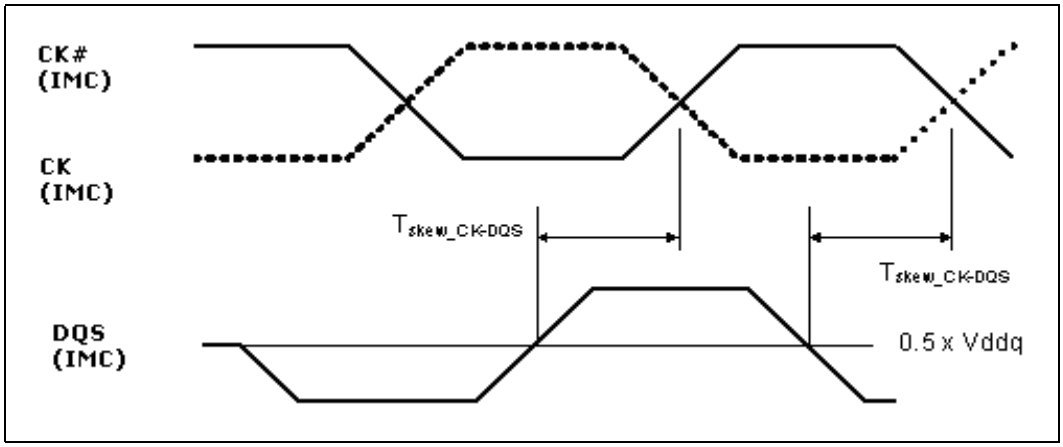
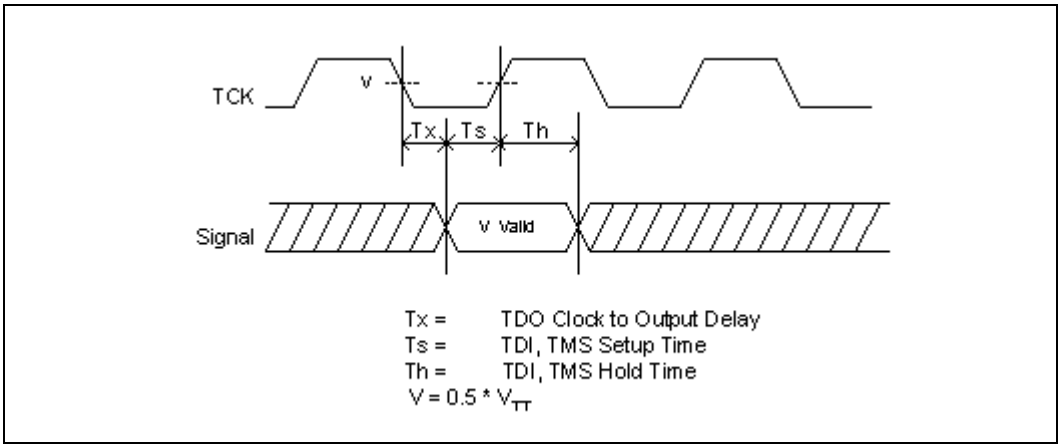


Figure 2-25. TAP Valid Delay Timing Waveform



Note: Please refer to Table 2-18 for TAP Signal Group DC specifications and Table 2-27 for TAP Signal Group AC specifications.

Figure 2-26. Test Reset (TRST#), Asynch GTL Input, and PROCHOT# Timing Waveform

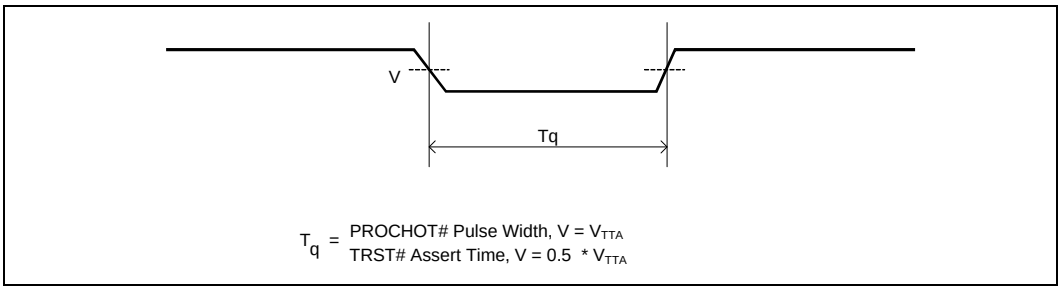


Figure 2-27. THERMTRIP# Power Down Sequence

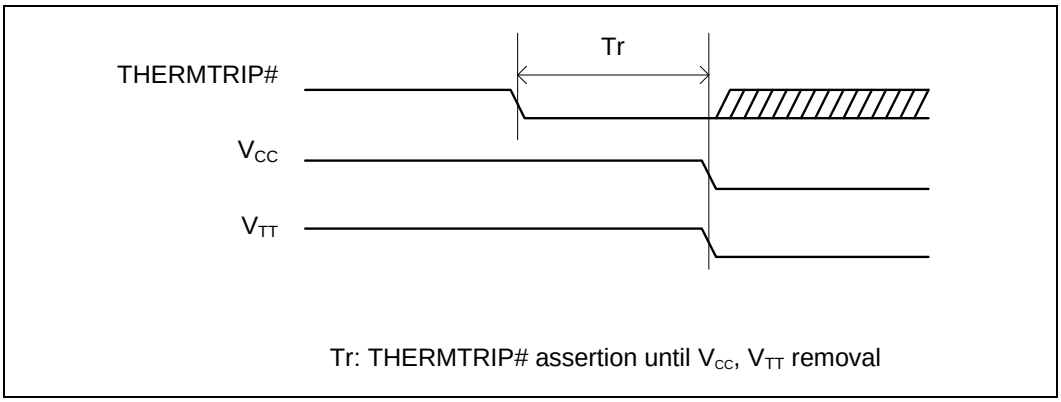
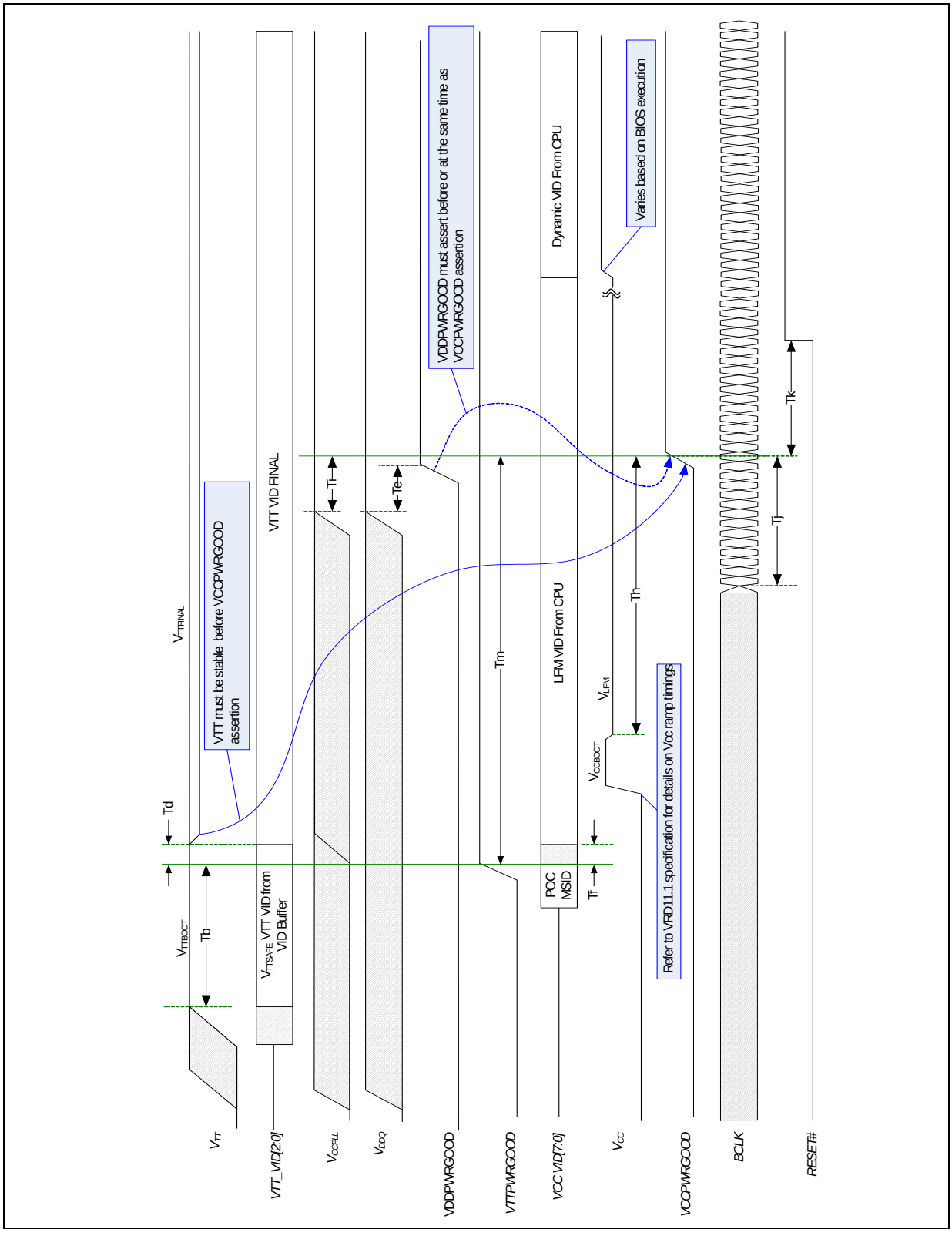
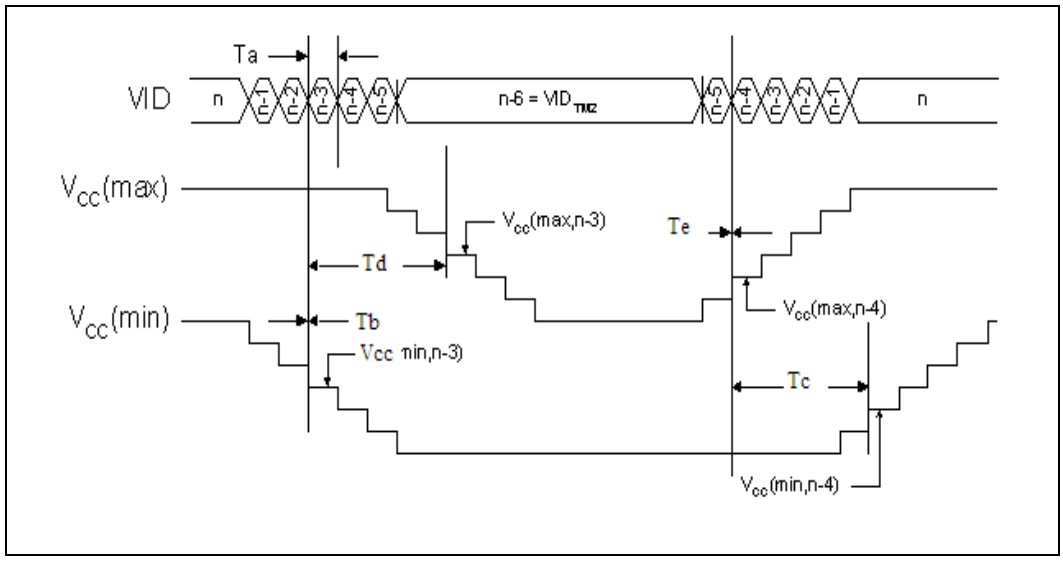


Figure 2-28. Voltage Sequence Timing Requirements



Note: In order In order to ensure Timestamp Counter (TSC) synchronization across sockets in multi-socket systems, the RESET# deassertion edge should arrive at the same BCLK rising edge at both sockets and should meet the Tsu and Th requirement of 600ps relative to BCLK, as outlined in Table 2-26.

Figure 2-29. VID Step Times and Vcc Waveforms



Note: This waveform illustrates an example of an Intel Adaptive Thermal Monitor transition or an Intel Enhanced SpeedStep Technology transition that is six VID step down from the current state and six steps back up. Any arbitrary up or down transition can be generalized from this waveform.

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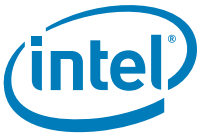
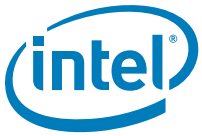




3 Signal Quality Specifications

Data transfer requires the clean reception of data and clock signals. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swings will adversely affect system timings. Ringback and signal non-monotonicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Overshoot and undershoot can also cause timing degradation due to the build up of inter-symbol interference (ISI) effects.

For these reasons, it is crucial that the designer work towards a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

This section documents signal quality metrics used to derive topology and routing guidelines through simulation. All specifications are specified at the processor die (pad measurements).

Specifications for signal quality are for measurements at the processor core only and are only observable through simulation. Therefore, proper signal simulation is the only means of properly verifying timing and signal quality requirements.

3.1 Overshoot/Undershoot Tolerance

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below V_{SS}. The overshoot/undershoot specifications limit transitions beyond V_{CCIO} or V_{SS} due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (that is, if the over/undershoot is great enough). Baseboard designs which meet signal integrity and timing requirements and which do not exceed the maximum overshoot or undershoot limits will insure reliable IO performance for the lifetime of the processor.

The pulse magnitude, duration, and activity factor must all be used to determine if the overshoot/undershoot pulse is within specifications.

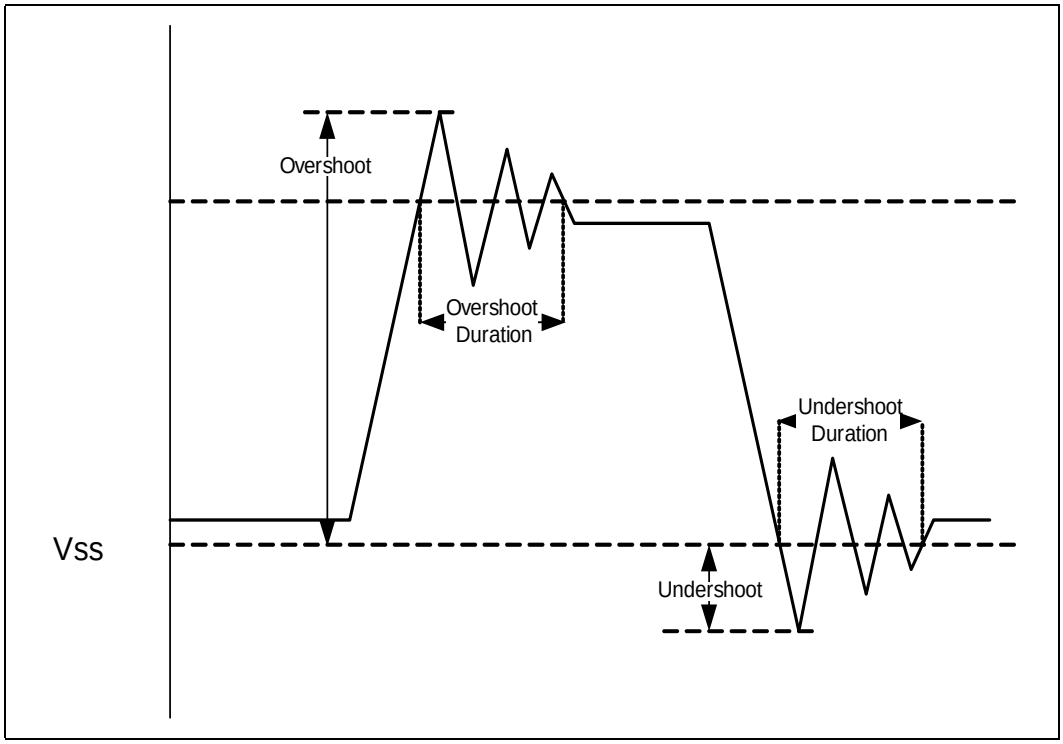
Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

Table 3-1. Overshoot/Undershoot Tolerance

Signal Group	Min Undershoot	Max Overshoot	Duration
Intel® QuickPath Interconnect	-0.1 * V_{TT}	1.2 * V_{TT}	500 ps
DDR3	-0.1 * V_{DDQ}	1.2 * V_{DDQ}	0.5 * T_{CH}
Processor Sideband Signals	-0.1 * V_{TT}	1.2 * V_{TT}	50 ns
System Reference Clock	-0.3	1.15	NA

Notes:
1. These specifications are measured at the processor pin.
2. Refer to Figure 3-1 for description of Overshoot/Undershoot magnitude and duration.

Figure 3-1. Maximum Acceptable Overshoot/Undershoot Waveform



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4 Package Mechanical Specifications

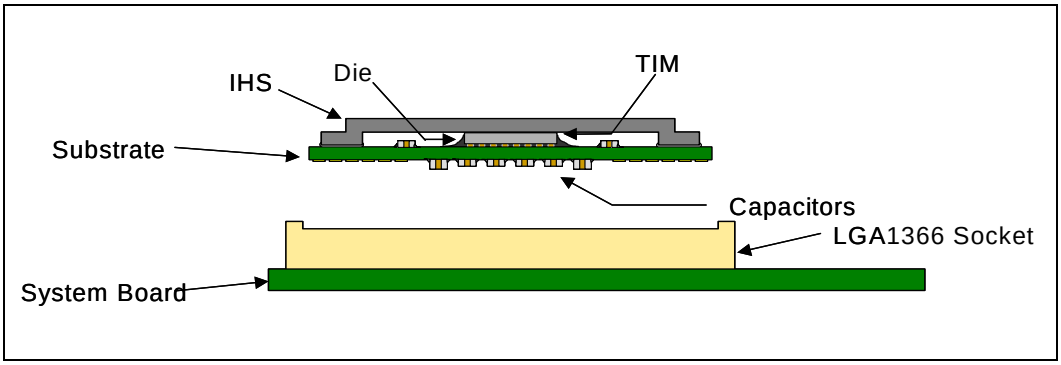
4.1 Package Mechanical Specifications

The processor is packaged in a Flip-Chip Land Grid Array (FC-LGA) package that interfaces with the baseboard via an LGA1366 socket. The package consists of a processor mounted on a substrate land-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor component thermal solutions, such as a heatsink. Figure 4-1 shows a sketch of the processor package components and how they are assembled together. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines)* for complete details on the LGA1366 socket.

The package components shown in Figure 4-1 include the following:

1. Integrated Heat Spreader (IHS)
2. Thermal Interface Material (TIM)
3. Processor core (die)
4. Package substrate
5. Capacitors

Figure 4-1. Processor Package Assembly Sketch



Note:
1. Socket and baseboard are included for reference and are not part of processor package.

4.1.1 Package Mechanical Drawing

The package mechanical drawings are shown in Figure 4-2 and Figure 4-3. The drawings include dimensions necessary to design a thermal solution and reflect the processor as received by Intel. These dimensions include:

1. Package reference with tolerances (total height, length, width, and so forth)
2. IHS parallelism and tilt
3. Land dimensions
4. Top-side and back-side component keep-out dimensions
5. Reference datums
6. All drawing dimensions are in mm.
7. Guidelines on potential IHS flatness variation with socket load plate actuation and installation of the cooling solution is available in the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines*.

Figure 4-2. Processor Package Drawing (Sheet 1 of 2)

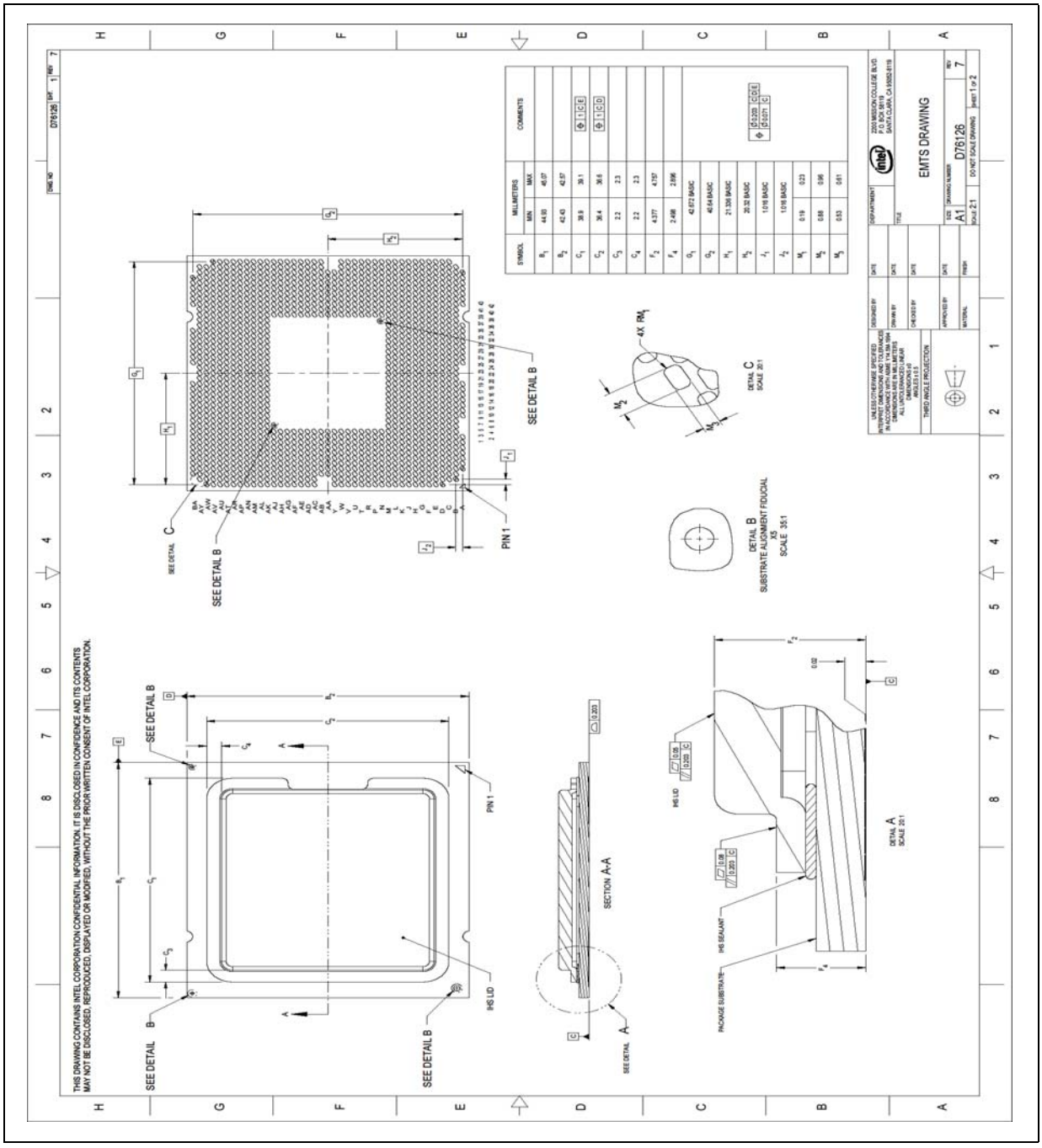
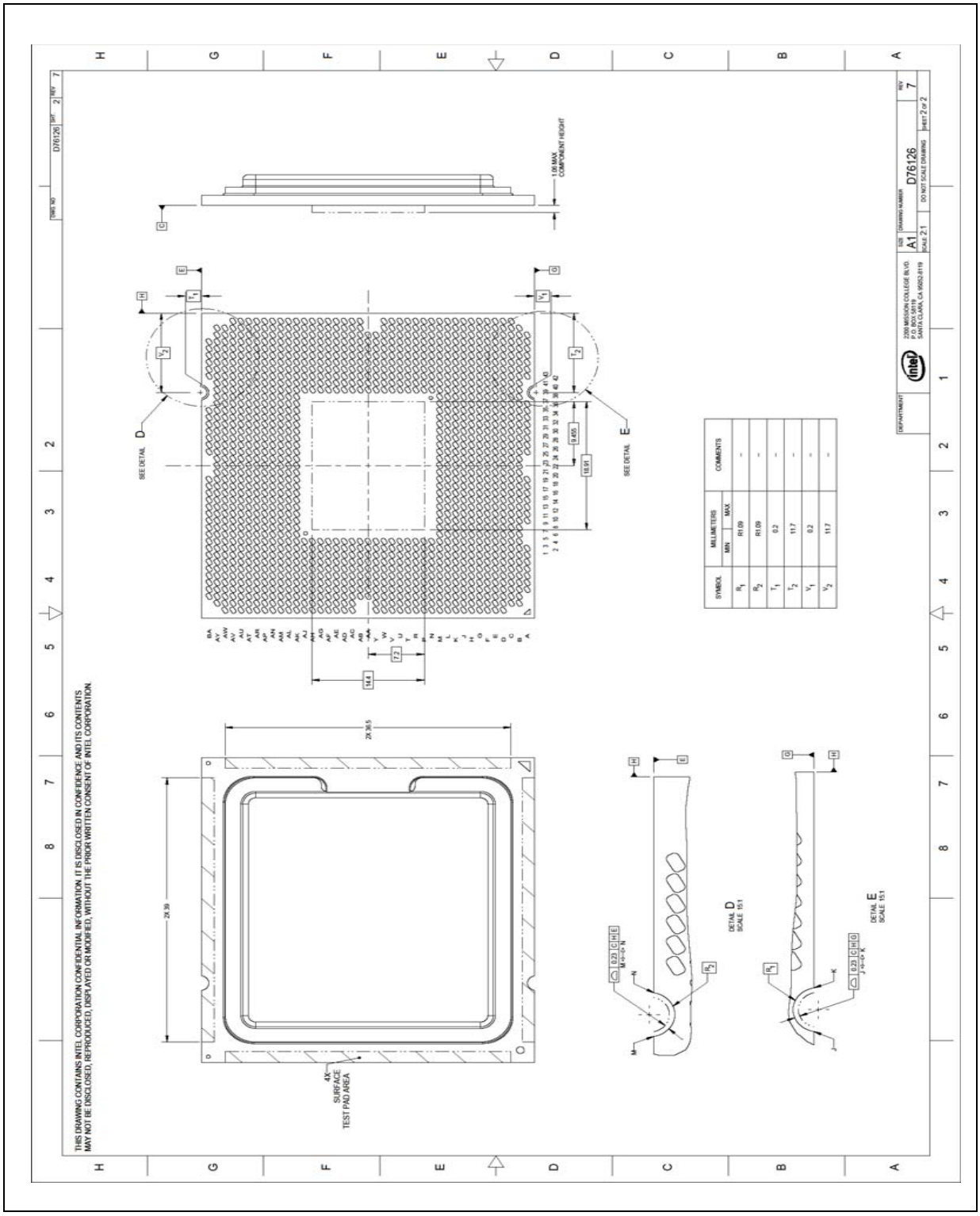
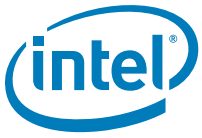


Figure 4-3. Processor Package Drawing (Sheet 2 of 2)





4.1.2 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Do not contact the Test Pad Area with conductive material. Decoupling capacitors are typically mounted to either the topside or land-side of the package substrate. See Figure 4-2 and Figure 4-3 for keep-out zones. The location and quantity of package capacitors may change due to manufacturing efficiencies but will remain within the component keep-in.

4.1.3 Package Loading Specifications

Table 4-1 provides load specifications for the processor package. These maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure. The processor substrate should not be used as a mechanical reference or load-bearing surface for thermal solutions.

Table 4-1. Processor Loading Specifications

Parameter	Maximum	Notes
Static Compressive Load	890 N [200 lbf]	1, 2, 3
Dynamic Compressive Load	1779 N [400 lbf] [max static compressive + dynamic load]	1, 3, 4

Notes:
1. These specifications apply to uniform compressive loading in a direction normal to the processor IHS.
2. This is the maximum static force that can be applied by the heatsink and Independent Loading Mechanism (ILM).
3. These specifications are based on limited testing for design characterization. Loading limits are for the package constrained by the limits of the processor socket.
4. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
5. See *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for minimum socket load to engage processor within socket.

4.1.4 Package Handling Guidelines

Table 4-2 includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

Table 4-2. Package Handling Guidelines

Parameter	Maximum Recommended	Notes
Shear	70 lbs	
Tensile	25 lbs	
Torque	35 in.lbs	

4.1.5 Package Insertion Specifications

The processor can be inserted into and removed from an LGA1366 socket 15 times. The socket should meet the LGA1366 requirements detailed in the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines*.

4.1.6 Processor Mass Specification

The typical mass of the processor is 35 grams. This mass [weight] includes all the components that are included in the package.

4.1.7 Processor Materials

Table 4-3 lists some of the package components and associated materials.

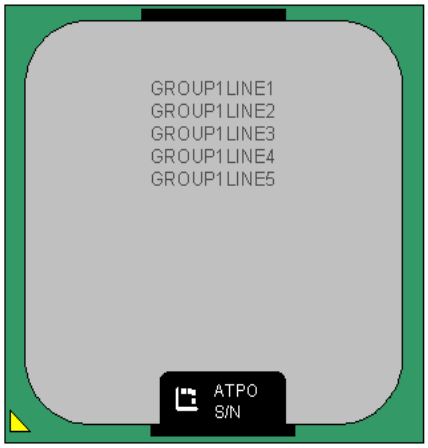
Table 4-3. Processor Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel Plated Copper
Substrate	Fiber Reinforced Resin
Substrate Lands	Gold Plated Copper

4.1.8 Processor Markings

Figure 4-4 shows the topside markings on the processor. This diagram is to aid in the identification of the processor.

Figure 4-4. Processor Top-Side Markings



Legend:	Mark Text (Production Mark):
GROUP1LINE1	
GROUP1LINE2	Intel ® Xeon®
GROUP1LINE3	Proc# SXXX COO
GROUP1LINE4	i (M) © '06
GROUP1LINE5	FPO e4

Legend:	Mark Text (Engineering Mark):
GROUP1LINE1	
GROUP1LINE2	INTEL CONFIDENTIAL
GROUP1LINE3	QXXX ES COO
GROUP1LINE4	i (M) © '06 80556KH0774M
GROUP1LINE5	FPO e4

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5 Land Listing

5.1 Listing by Land Name

Table 5-1. By Land Name (Sheet 1 of 36)

Land Name	Land No.	Buffer Type	Direction
BCLK_DN	AH35	CMOS	I
BCLK_DP	AJ35	CMOS	I
BCLK_ITP_DN	AA4	CMOS	O
BCLK_ITP_DP	AA5	CMOS	O
BPM#[0]	B3	GTL	I/O
BPM#[1]	A5	GTL	I/O
BPM#[2]	C2	GTL	I/O
BPM#[3]	B4	GTL	I/O
BPM#[4]	D1	GTL	I/O
BPM#[5]	C3	GTL	I/O
BPM#[6]	D2	GTL	I/O
BPM#[7]	E2	GTL	I/O
CAT_ERR#	AC37	GTL	I/O
COMP0	AB41	Analog	
QPI0_CLKRX_DN	AR42	QPI	I
QPI0_CLKRX_DP	AR41	QPI	I
QPI0_CLKTX_DN	AF42	QPI	O
QPI0_CLKTX_DP	AG42	QPI	O
QPI0_COMP	AL43	Analog	
QPI0_DRX_DN[0]	AU37	QPI	I
QPI0_DRX_DN[1]	AV38	QPI	I
QPI0_DRX_DN[10]	AT42	QPI	I
QPI0_DRX_DN[11]	AR43	QPI	I
QPI0_DRX_DN[12]	AR40	QPI	I
QPI0_DRX_DN[13]	AN42	QPI	I
QPI0_DRX_DN[14]	AM43	QPI	I
QPI0_DRX_DN[15]	AM40	QPI	I
QPI0_DRX_DN[16]	AM41	QPI	I
QPI0_DRX_DN[17]	AP40	QPI	I
QPI0_DRX_DN[18]	AP39	QPI	I
QPI0_DRX_DN[19]	AR38	QPI	I
QPI0_DRX_DN[2]	AV37	QPI	I
QPI0_DRX_DN[3]	AY36	QPI	I
QPI0_DRX_DN[4]	BA37	QPI	I
QPI0_DRX_DN[5]	AW38	QPI	I

Table 5-1. By Land Name (Sheet 2 of 36)

Land Name	Land No.	Buffer Type	Direction
QPI0_DRX_DN[6]	AY38	QPI	I
QPI0_DRX_DN[7]	AT39	QPI	I
QPI0_DRX_DN[8]	AV40	QPI	I
QPI0_DRX_DN[9]	AU41	QPI	I
QPI0_DRX_DP[0]	AT37	QPI	I
QPI0_DRX_DP[1]	AU38	QPI	I
QPI0_DRX_DP[10]	AU42	QPI	I
QPI0_DRX_DP[11]	AT43	QPI	I
QPI0_DRX_DP[12]	AT40	QPI	I
QPI0_DRX_DP[13]	AP42	QPI	I
QPI0_DRX_DP[14]	AN43	QPI	I
QPI0_DRX_DP[15]	AN40	QPI	I
QPI0_DRX_DP[16]	AM42	QPI	I
QPI0_DRX_DP[17]	AP41	QPI	I
QPI0_DRX_DP[18]	AN39	QPI	I
QPI0_DRX_DP[19]	AP38	QPI	I
QPI0_DRX_DP[2]	AV36	QPI	I
QPI0_DRX_DP[3]	AW36	QPI	I
QPI0_DRX_DP[4]	BA36	QPI	I
QPI0_DRX_DP[5]	AW37	QPI	I
QPI0_DRX_DP[6]	BA38	QPI	I
QPI0_DRX_DP[7]	AU39	QPI	I
QPI0_DRX_DP[8]	AW40	QPI	I
QPI0_DRX_DP[9]	AU40	QPI	I
QPI0_DTX_DN[0]	AH38	QPI	O
QPI0_DTX_DN[1]	AG39	QPI	O
QPI0_DTX_DN[10]	AE43	QPI	O
QPI0_DTX_DN[11]	AE41	QPI	O
QPI0_DTX_DN[12]	AC42	QPI	O
QPI0_DTX_DN[13]	AB43	QPI	O
QPI0_DTX_DN[14]	AD39	QPI	O
QPI0_DTX_DN[15]	AC40	QPI	O
QPI0_DTX_DN[16]	AC38	QPI	O
QPI0_DTX_DN[17]	AB38	QPI	O
QPI0_DTX_DN[18]	AE38	QPI	O
QPI0_DTX_DN[19]	AF40	QPI	O

Table 5-1. By Land Name (Sheet 3 of 36)

Land Name	Land No.	Buffer Type	Direction
QPI0_DTX_DN[2]	AK38	QPI	O
QPI0_DTX_DN[3]	AJ39	QPI	O
QPI0_DTX_DN[4]	AJ40	QPI	O
QPI0_DTX_DN[5]	AK41	QPI	O
QPI0_DTX_DN[6]	AH42	QPI	O
QPI0_DTX_DN[7]	AJ42	QPI	O
QPI0_DTX_DN[8]	AH43	QPI	O
QPI0_DTX_DN[9]	AG41	QPI	O
QPI0_DTX_DP[0]	AG38	QPI	O
QPI0_DTX_DP[1]	AF39	QPI	O
QPI0_DTX_DP[10]	AF43	QPI	O
QPI0_DTX_DP[11]	AE42	QPI	O
QPI0_DTX_DP[12]	AD42	QPI	O
QPI0_DTX_DP[13]	AC43	QPI	O
QPI0_DTX_DP[14]	AD40	QPI	O
QPI0_DTX_DP[15]	AC41	QPI	O
QPI0_DTX_DP[16]	AC39	QPI	O
QPI0_DTX_DP[17]	AB39	QPI	O
QPI0_DTX_DP[18]	AD38	QPI	O
QPI0_DTX_DP[19]	AE40	QPI	O
QPI0_DTX_DP[2]	AK37	QPI	O
QPI0_DTX_DP[3]	AJ38	QPI	O
QPI0_DTX_DP[4]	AH40	QPI	O
QPI0_DTX_DP[5]	AK40	QPI	O
QPI0_DTX_DP[6]	AH41	QPI	O
QPI0_DTX_DP[7]	AK42	QPI	O
QPI0_DTX_DP[8]	AJ43	QPI	O
QPI0_DTX_DP[9]	AG40	QPI	O
QPI1_CLKRX_DN	AR6	QPI	I
QPI1_CLKRX_DP	AT6	QPI	I
QPI1_CLKTX_DN	AE6	QPI	O
QPI1_CLKTX_DP	AF6	QPI	O
QPI1_COMP	AL6	Analog	
QPI1_DRX_DN[0]	AV8	QPI	I
QPI1_DRX_DN[1]	AW7	QPI	I
QPI1_DRX_DN[10]	AR1	QPI	I
QPI1_DRX_DN[11]	AR5	QPI	I
QPI1_DRX_DN[12]	AN2	QPI	I
QPI1_DRX_DN[13]	AM1	QPI	I
QPI1_DRX_DN[14]	AM3	QPI	I
QPI1_DRX_DN[15]	AP4	QPI	I

Table 5-1. By Land Name (Sheet 4 of 36)

Land Name	Land No.	Buffer Type	Direction
QPI1_DRX_DN[16]	AN4	QPI	I
QPI1_DRX_DN[17]	AN6	QPI	I
QPI1_DRX_DN[18]	AM7	QPI	I
QPI1_DRX_DN[19]	AL8	QPI	I
QPI1_DRX_DN[2]	BA8	QPI	I
QPI1_DRX_DN[3]	AW5	QPI	I
QPI1_DRX_DN[4]	BA6	QPI	I
QPI1_DRX_DN[5]	AY5	QPI	I
QPI1_DRX_DN[6]	AU6	QPI	I
QPI1_DRX_DN[7]	AW3	QPI	I
QPI1_DRX_DN[8]	AU3	QPI	I
QPI1_DRX_DN[9]	AT2	QPI	I
QPI1_DRX_DP[0]	AU8	QPI	I
QPI1_DRX_DP[1]	AV7	QPI	I
QPI1_DRX_DP[10]	AT1	QPI	I
QPI1_DRX_DP[11]	AR4	QPI	I
QPI1_DRX_DP[12]	AP2	QPI	I
QPI1_DRX_DP[13]	AN1	QPI	I
QPI1_DRX_DP[14]	AM2	QPI	I
QPI1_DRX_DP[15]	AP3	QPI	I
QPI1_DRX_DP[16]	AM4	QPI	I
QPI1_DRX_DP[17]	AN5	QPI	I
QPI1_DRX_DP[18]	AM6	QPI	I
QPI1_DRX_DP[19]	AM8	QPI	I
QPI1_DRX_DP[2]	AY8	QPI	I
QPI1_DRX_DP[3]	AV5	QPI	I
QPI1_DRX_DP[4]	BA7	QPI	I
QPI1_DRX_DP[5]	AY6	QPI	I
QPI1_DRX_DP[6]	AU7	QPI	I
QPI1_DRX_DP[7]	AW4	QPI	I
QPI1_DRX_DP[8]	AU4	QPI	I
QPI1_DRX_DP[9]	AT3	QPI	I
QPI1_DTX_DN[0]	AH8	QPI	O
QPI1_DTX_DN[1]	AJ7	QPI	O
QPI1_DTX_DN[10]	AF3	QPI	O
QPI1_DTX_DN[11]	AD1	QPI	O
QPI1_DTX_DN[12]	AD3	QPI	O
QPI1_DTX_DN[13]	AB3	QPI	O
QPI1_DTX_DN[14]	AE4	QPI	O
QPI1_DTX_DN[15]	AD4	QPI	O
QPI1_DTX_DN[16]	AC6	QPI	O

Table 5-1. By Land Name (Sheet 5 of 36)

Land Name	Land No.	Buffer Type	Direction
QPI1_DTX_DN[17]	AD7	QPI	O
QPI1_DTX_DN[18]	AE5	QPI	O
QPI1_DTX_DN[19]	AD8	QPI	O
QPI1_DTX_DN[2]	AJ6	QPI	O
QPI1_DTX_DN[3]	AK5	QPI	O
QPI1_DTX_DN[4]	AK4	QPI	O
QPI1_DTX_DN[5]	AG6	QPI	O
QPI1_DTX_DN[6]	AJ2	QPI	O
QPI1_DTX_DN[7]	AJ1	QPI	O
QPI1_DTX_DN[8]	AH4	QPI	O
QPI1_DTX_DN[9]	AG2	QPI	O
QPI1_DTX_DP[0]	AG8	QPI	O
QPI1_DTX_DP[1]	AJ8	QPI	O
QPI1_DTX_DP[10]	AF2	QPI	O
QPI1_DTX_DP[11]	AE1	QPI	O
QPI1_DTX_DP[12]	AD2	QPI	O
QPI1_DTX_DP[13]	AC3	QPI	O
QPI1_DTX_DP[14]	AE3	QPI	O
QPI1_DTX_DP[15]	AC4	QPI	O
QPI1_DTX_DP[16]	AB6	QPI	O
QPI1_DTX_DP[17]	AD6	QPI	O
QPI1_DTX_DP[18]	AD5	QPI	O
QPI1_DTX_DP[19]	AC8	QPI	O
QPI1_DTX_DP[2]	AH6	QPI	O
QPI1_DTX_DP[3]	AK6	QPI	O
QPI1_DTX_DP[4]	AJ4	QPI	O
QPI1_DTX_DP[5]	AG7	QPI	O
QPI1_DTX_DP[6]	AJ3	QPI	O
QPI1_DTX_DP[7]	AK1	QPI	O
QPI1_DTX_DP[8]	AH3	QPI	O
QPI1_DTX_DP[9]	AH2	QPI	O
DBR#	AF10	Asynch	I
DDR_COMP[0]	AA8	Analog	
DDR_COMP[1]	Y7	Analog	
DDR_COMP[2]	AC1	Analog	
DDR_THERM#	AB5	CMOS	I
DDR_THERM2#	AF4	CMOS	I
DDR_VREF	L23	Analog	I
DDR0_BA[0]	B16	CMOS	O
DDR0_BA[1]	A16	CMOS	O
DDR0_BA[2]	C28	CMOS	O

Table 5-1. By Land Name (Sheet 6 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR0_CAS#	C12	CMOS	O
DDR0_CKE[0]	C29	CMOS	O
DDR0_CKE[1]	A30	CMOS	O
DDR0_CKE[2]	B30	CMOS	O
DDR0_CKE[3]	B31	CMOS	O
DDR0_CLK_N[0]	K19	CLOCK	O
DDR0_CLK_N[1]	C19	CLOCK	O
DDR0_CLK_N[2]	E18	CLOCK	O
DDR0_CLK_N[3]	E19	CLOCK	O
DDR0_CLK_P[0]	J19	CLOCK	O
DDR0_CLK_P[1]	D19	CLOCK	O
DDR0_CLK_P[2]	F18	CLOCK	O
DDR0_CLK_P[3]	E20	CLOCK	O
DDR0_CS#[0]	G15	CMOS	O
DDR0_CS#[1]	B10	CMOS	O
DDR0_CS#[2]	C13	CMOS	O
DDR0_CS#[3]	B9	CMOS	O
DDR0_CS#[4]	B15	CMOS	O
DDR0_CS#[5]	A7	CMOS	O
DDR0_CS#[6]/ DDR0_ODT[4]	C11	CMOS	O
DDR0_CS#[7]/ DDR0_ODT[5]	B8	CMOS	O
DDR0_DQ[0]	W41	CMOS	I/O
DDR0_DQ[1]	V41	CMOS	I/O
DDR0_DQ[10]	K42	CMOS	I/O
DDR0_DQ[11]	K43	CMOS	I/O
DDR0_DQ[12]	P42	CMOS	I/O
DDR0_DQ[13]	P41	CMOS	I/O
DDR0_DQ[14]	L43	CMOS	I/O
DDR0_DQ[15]	L42	CMOS	I/O
DDR0_DQ[16]	H41	CMOS	I/O
DDR0_DQ[17]	H43	CMOS	I/O
DDR0_DQ[18]	E42	CMOS	I/O
DDR0_DQ[19]	E43	CMOS	I/O
DDR0_DQ[2]	R43	CMOS	I/O
DDR0_DQ[20]	J42	CMOS	I/O
DDR0_DQ[21]	J41	CMOS	I/O
DDR0_DQ[22]	F43	CMOS	I/O
DDR0_DQ[23]	F42	CMOS	I/O
DDR0_DQ[24]	D40	CMOS	I/O
DDR0_DQ[25]	C41	CMOS	I/O

Table 5-1. By Land Name (Sheet 7 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR0_DQ[26]	A38	CMOS	I/O
DDR0_DQ[27]	D37	CMOS	I/O
DDR0_DQ[28]	D41	CMOS	I/O
DDR0_DQ[29]	D42	CMOS	I/O
DDR0_DQ[3]	R42	CMOS	I/O
DDR0_DQ[30]	C38	CMOS	I/O
DDR0_DQ[31]	B38	CMOS	I/O
DDR0_DQ[32]	B5	CMOS	I/O
DDR0_DQ[33]	C4	CMOS	I/O
DDR0_DQ[34]	F1	CMOS	I/O
DDR0_DQ[35]	G3	CMOS	I/O
DDR0_DQ[36]	B6	CMOS	I/O
DDR0_DQ[37]	C6	CMOS	I/O
DDR0_DQ[38]	F3	CMOS	I/O
DDR0_DQ[39]	F2	CMOS	I/O
DDR0_DQ[4]	W40	CMOS	I/O
DDR0_DQ[40]	H2	CMOS	I/O
DDR0_DQ[41]	H1	CMOS	I/O
DDR0_DQ[42]	L1	CMOS	I/O
DDR0_DQ[43]	M1	CMOS	I/O
DDR0_DQ[44]	G1	CMOS	I/O
DDR0_DQ[45]	H3	CMOS	I/O
DDR0_DQ[46]	L3	CMOS	I/O
DDR0_DQ[47]	L2	CMOS	I/O
DDR0_DQ[48]	N1	CMOS	I/O
DDR0_DQ[49]	N2	CMOS	I/O
DDR0_DQ[5]	W42	CMOS	I/O
DDR0_DQ[50]	T1	CMOS	I/O
DDR0_DQ[51]	T2	CMOS	I/O
DDR0_DQ[52]	M3	CMOS	I/O
DDR0_DQ[53]	N3	CMOS	I/O
DDR0_DQ[54]	R4	CMOS	I/O
DDR0_DQ[55]	T3	CMOS	I/O
DDR0_DQ[56]	U4	CMOS	I/O
DDR0_DQ[57]	V1	CMOS	I/O
DDR0_DQ[58]	Y2	CMOS	I/O
DDR0_DQ[59]	Y3	CMOS	I/O
DDR0_DQ[6]	U41	CMOS	I/O
DDR0_DQ[60]	U1	CMOS	I/O
DDR0_DQ[61]	U3	CMOS	I/O
DDR0_DQ[62]	V4	CMOS	I/O

Table 5-1. By Land Name (Sheet 8 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR0_DQ[63]	W4	CMOS	I/O
DDR0_DQ[7]	T42	CMOS	I/O
DDR0_DQ[8]	N41	CMOS	I/O
DDR0_DQ[9]	N43	CMOS	I/O
DDR0_DQS_N[0]	U43	CMOS	I/O
DDR0_DQS_N[1]	M41	CMOS	I/O
DDR0_DQS_N[10]	M43	CMOS	I/O
DDR0_DQS_N[11]	G43	CMOS	I/O
DDR0_DQS_N[12]	C39	CMOS	I/O
DDR0_DQS_N[13]	D4	CMOS	I/O
DDR0_DQS_N[14]	J1	CMOS	I/O
DDR0_DQS_N[15]	P1	CMOS	I/O
DDR0_DQS_N[16]	V3	CMOS	I/O
DDR0_DQS_N[17]	B35	CMOS	I/O
DDR0_DQS_N[2]	G41	CMOS	I/O
DDR0_DQS_N[3]	B40	CMOS	I/O
DDR0_DQS_N[4]	E4	CMOS	I/O
DDR0_DQS_N[5]	K3	CMOS	I/O
DDR0_DQS_N[6]	R3	CMOS	I/O
DDR0_DQS_N[7]	W1	CMOS	I/O
DDR0_DQS_N[8]	D35	CMOS	I/O
DDR0_DQS_N[9]	V42	CMOS	I/O
DDR0_DQS_P[0]	T43	CMOS	I/O
DDR0_DQS_P[1]	L41	CMOS	I/O
DDR0_DQS_P[10]	N42	CMOS	I/O
DDR0_DQS_P[11]	H42	CMOS	I/O
DDR0_DQS_P[12]	D39	CMOS	I/O
DDR0_DQS_P[13]	D5	CMOS	I/O
DDR0_DQS_P[14]	J2	CMOS	I/O
DDR0_DQS_P[15]	P2	CMOS	I/O
DDR0_DQS_P[16]	V2	CMOS	I/O
DDR0_DQS_P[17]	B36	CMOS	I/O
DDR0_DQS_P[2]	F41	CMOS	I/O
DDR0_DQS_P[3]	B39	CMOS	I/O
DDR0_DQS_P[4]	E3	CMOS	I/O
DDR0_DQS_P[5]	K2	CMOS	I/O
DDR0_DQS_P[6]	R2	CMOS	I/O
DDR0_DQS_P[7]	W2	CMOS	I/O
DDR0_DQS_P[8]	D34	CMOS	I/O
DDR0_DQS_P[9]	V43	CMOS	I/O
DDR0_ECC[0]	C36	CMOS	I/O

Table 5-1. By Land Name (Sheet 9 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR0_ECC[1]	A36	CMOS	I/O
DDR0_ECC[2]	F32	CMOS	I/O
DDR0_ECC[3]	C33	CMOS	I/O
DDR0_ECC[4]	C37	CMOS	I/O
DDR0_ECC[5]	A37	CMOS	I/O
DDR0_ECC[6]	B34	CMOS	I/O
DDR0_ECC[7]	C34	CMOS	I/O
DDR0_MA[0]	A20	CMOS	O
DDR0_MA[1]	B21	CMOS	O
DDR0_MA[10]	B19	CMOS	O
DDR0_MA[11]	A26	CMOS	O
DDR0_MA[12]	B26	CMOS	O
DDR0_MA[13]	A10	CMOS	O
DDR0_MA[14]	A28	CMOS	O
DDR0_MA[15]	B29	CMOS	O
DDR0_MA[2]	C23	CMOS	O
DDR0_MA[3]	D24	CMOS	O
DDR0_MA[4]	B23	CMOS	O
DDR0_MA[5]	B24	CMOS	O
DDR0_MA[6]	C24	CMOS	O
DDR0_MA[7]	A25	CMOS	O
DDR0_MA[8]	B25	CMOS	O
DDR0_MA[9]	C26	CMOS	O
DDR0_MA_PAR	B20	CMOS	O
DDR0_ODT[0]	F12	CMOS	O
DDR0_ODT[1]	C9	CMOS	O
DDR0_ODT[2]	B11	CMOS	O
DDR0_ODT[3]	C7	CMOS	O
DDR0_PAR_ERR#[0]	D25	Asynch	I
DDR0_PAR_ERR#[1]	B28	Asynch	I
DDR0_PAR_ERR#[2]	A27	Asynch	I
DDR0_RAS#	A15	CMOS	O
DDR0_RESET#	D32	CMOS	O
DDR0_WE#	B13	CMOS	O
DDR1_BA[0]	C18	CMOS	O
DDR1_BA[1]	K13	CMOS	O
DDR1_BA[2]	H27	CMOS	O
DDR1_CAS#	E14	CMOS	O
DDR1_CKE[0]	H28	CMOS	O
DDR1_CKE[1]	E27	CMOS	O
DDR1_CKE[2]	D27	CMOS	O

Table 5-1. By Land Name (Sheet 10 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR1_CKE[3]	C27	CMOS	O
DDR1_CLK_N[0]	D21	CLOCK	O
DDR1_CLK_N[1]	G20	CLOCK	O
DDR1_CLK_N[2]	L18	CLOCK	O
DDR1_CLK_N[3]	H19	CLOCK	O
DDR1_CLK_P[0]	C21	CLOCK	O
DDR1_CLK_P[1]	G19	CLOCK	O
DDR1_CLK_P[2]	K18	CLOCK	O
DDR1_CLK_P[3]	H18	CLOCK	O
DDR1_CS#[0]	D12	CMOS	O
DDR1_CS#[1]	A8	CMOS	O
DDR1_CS#[2]	E15	CMOS	O
DDR1_CS#[3]	E13	CMOS	O
DDR1_CS#[4]	C17	CMOS	O
DDR1_CS#[5]	E10	CMOS	O
DDR1_CS#[6]/ DDR1_ODT[4]	C14	CMOS	O
DDR1_CS#[7]/ DDR1_ODT[5]	E12	CMOS	O
DDR1_DQ[0]	AA37	CMOS	I/O
DDR1_DQ[1]	AA36	CMOS	I/O
DDR1_DQ[10]	P39	CMOS	I/O
DDR1_DQ[11]	N39	CMOS	I/O
DDR1_DQ[12]	R34	CMOS	I/O
DDR1_DQ[13]	R35	CMOS	I/O
DDR1_DQ[14]	N37	CMOS	I/O
DDR1_DQ[15]	N38	CMOS	I/O
DDR1_DQ[16]	M35	CMOS	I/O
DDR1_DQ[17]	M34	CMOS	I/O
DDR1_DQ[18]	K35	CMOS	I/O
DDR1_DQ[19]	J35	CMOS	I/O
DDR1_DQ[2]	Y35	CMOS	I/O
DDR1_DQ[20]	N34	CMOS	I/O
DDR1_DQ[21]	M36	CMOS	I/O
DDR1_DQ[22]	J36	CMOS	I/O
DDR1_DQ[23]	H36	CMOS	I/O
DDR1_DQ[24]	H33	CMOS	I/O
DDR1_DQ[25]	L33	CMOS	I/O
DDR1_DQ[26]	K32	CMOS	I/O
DDR1_DQ[27]	J32	CMOS	I/O
DDR1_DQ[28]	J34	CMOS	I/O
DDR1_DQ[29]	H34	CMOS	I/O

Table 5-1. By Land Name (Sheet 11 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR1_DQ[3]	Y34	CMOS	I/O
DDR1_DQ[30]	L32	CMOS	I/O
DDR1_DQ[31]	K30	CMOS	I/O
DDR1_DQ[32]	E9	CMOS	I/O
DDR1_DQ[33]	E8	CMOS	I/O
DDR1_DQ[34]	E5	CMOS	I/O
DDR1_DQ[35]	F5	CMOS	I/O
DDR1_DQ[36]	F10	CMOS	I/O
DDR1_DQ[37]	G8	CMOS	I/O
DDR1_DQ[38]	D6	CMOS	I/O
DDR1_DQ[39]	F6	CMOS	I/O
DDR1_DQ[4]	AA35	CMOS	I/O
DDR1_DQ[40]	H8	CMOS	I/O
DDR1_DQ[41]	J6	CMOS	I/O
DDR1_DQ[42]	G4	CMOS	I/O
DDR1_DQ[43]	H4	CMOS	I/O
DDR1_DQ[44]	G9	CMOS	I/O
DDR1_DQ[45]	H9	CMOS	I/O
DDR1_DQ[46]	G5	CMOS	I/O
DDR1_DQ[47]	J5	CMOS	I/O
DDR1_DQ[48]	K4	CMOS	I/O
DDR1_DQ[49]	K5	CMOS	I/O
DDR1_DQ[5]	AB36	CMOS	I/O
DDR1_DQ[50]	R5	CMOS	I/O
DDR1_DQ[51]	T5	CMOS	I/O
DDR1_DQ[52]	J4	CMOS	I/O
DDR1_DQ[53]	M6	CMOS	I/O
DDR1_DQ[54]	R8	CMOS	I/O
DDR1_DQ[55]	R7	CMOS	I/O
DDR1_DQ[56]	W6	CMOS	I/O
DDR1_DQ[57]	W7	CMOS	I/O
DDR1_DQ[58]	Y10	CMOS	I/O
DDR1_DQ[59]	W10	CMOS	I/O
DDR1_DQ[6]	Y40	CMOS	I/O
DDR1_DQ[60]	V9	CMOS	I/O
DDR1_DQ[61]	W5	CMOS	I/O
DDR1_DQ[62]	AA7	CMOS	I/O
DDR1_DQ[63]	W9	CMOS	I/O
DDR1_DQ[7]	Y39	CMOS	I/O
DDR1_DQ[8]	P34	CMOS	I/O
DDR1_DQ[9]	P35	CMOS	I/O

Table 5-1. By Land Name (Sheet 12 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR1_DQS_N[0]	Y37	CMOS	I/O
DDR1_DQS_N[1]	R37	CMOS	I/O
DDR1_DQS_N[10]	P37	CMOS	I/O
DDR1_DQS_N[11]	K37	CMOS	I/O
DDR1_DQS_N[12]	K33	CMOS	I/O
DDR1_DQS_N[13]	F7	CMOS	I/O
DDR1_DQS_N[14]	J7	CMOS	I/O
DDR1_DQS_N[15]	M4	CMOS	I/O
DDR1_DQS_N[16]	Y5	CMOS	I/O
DDR1_DQS_N[17]	E35	CMOS	I/O
DDR1_DQS_N[2]	L36	CMOS	I/O
DDR1_DQS_N[3]	L31	CMOS	I/O
DDR1_DQS_N[4]	D7	CMOS	I/O
DDR1_DQS_N[5]	G6	CMOS	I/O
DDR1_DQS_N[6]	L5	CMOS	I/O
DDR1_DQS_N[7]	Y9	CMOS	I/O
DDR1_DQS_N[8]	G34	CMOS	I/O
DDR1_DQS_N[9]	AA41	CMOS	I/O
DDR1_DQS_P[0]	Y38	CMOS	I/O
DDR1_DQS_P[1]	R38	CMOS	I/O
DDR1_DQS_P[10]	P36	CMOS	I/O
DDR1_DQS_P[11]	L37	CMOS	I/O
DDR1_DQS_P[12]	K34	CMOS	I/O
DDR1_DQS_P[13]	F8	CMOS	I/O
DDR1_DQS_P[14]	H7	CMOS	I/O
DDR1_DQS_P[15]	M5	CMOS	I/O
DDR1_DQS_P[16]	Y4	CMOS	I/O
DDR1_DQS_P[17]	F35	CMOS	I/O
DDR1_DQS_P[2]	L35	CMOS	I/O
DDR1_DQS_P[3]	L30	CMOS	I/O
DDR1_DQS_P[4]	E7	CMOS	I/O
DDR1_DQS_P[5]	H6	CMOS	I/O
DDR1_DQS_P[6]	L6	CMOS	I/O
DDR1_DQS_P[7]	Y8	CMOS	I/O
DDR1_DQS_P[8]	G33	CMOS	I/O
DDR1_DQS_P[9]	AA40	CMOS	I/O
DDR1_ECC[0]	D36	CMOS	I/O
DDR1_ECC[1]	F36	CMOS	I/O
DDR1_ECC[2]	E33	CMOS	I/O
DDR1_ECC[3]	G36	CMOS	I/O
DDR1_ECC[4]	E37	CMOS	I/O

Table 5-1. By Land Name (Sheet 13 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR1_ECC[5]	F37	CMOS	I/O
DDR1_ECC[6]	E34	CMOS	I/O
DDR1_ECC[7]	G35	CMOS	I/O
DDR1_MA[0]	J14	CMOS	O
DDR1_MA[1]	J16	CMOS	O
DDR1_MA[10]	H14	CMOS	O
DDR1_MA[11]	E23	CMOS	O
DDR1_MA[12]	E24	CMOS	O
DDR1_MA[13]	B14	CMOS	O
DDR1_MA[14]	H26	CMOS	O
DDR1_MA[15]	F26	CMOS	O
DDR1_MA[2]	J17	CMOS	O
DDR1_MA[3]	L28	CMOS	O
DDR1_MA[4]	K28	CMOS	O
DDR1_MA[5]	F22	CMOS	O
DDR1_MA[6]	J27	CMOS	O
DDR1_MA[7]	D22	CMOS	O
DDR1_MA[8]	E22	CMOS	O
DDR1_MA[9]	G24	CMOS	O
DDR1_MA_PAR	D20	CMOS	O
DDR1_ODT[0]	D11	CMOS	O
DDR1_ODT[1]	C8	CMOS	O
DDR1_ODT[2]	D14	CMOS	O
DDR1_ODT[3]	F11	CMOS	O
DDR1_PAR_ERR#[0]	C22	Asynch	I
DDR1_PAR_ERR#[1]	E25	Asynch	I
DDR1_PAR_ERR#[2]	F25	Asynch	I
DDR1_RAS#	G14	CMOS	O
DDR1_RESET#	D29	CMOS	O
DDR1_WE#	G13	CMOS	O
DDR2_BA[0]	A17	CMOS	O
DDR2_BA[1]	F17	CMOS	O
DDR2_BA[2]	L26	CMOS	O
DDR2_CAS#	F16	CMOS	O
DDR2_CKE[0]	J26	CMOS	O
DDR2_CKE[1]	G26	CMOS	O
DDR2_CKE[2]	D26	CMOS	O
DDR2_CKE[3]	L27	CMOS	O
DDR2_CLK_N[0]	J21	CLOCK	O
DDR2_CLK_N[1]	K20	CLOCK	O
DDR2_CLK_N[2]	G21	CLOCK	O

Table 5-1. By Land Name (Sheet 14 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR2_CLK_N[3]	L21	CLOCK	O
DDR2_CLK_P[0]	J22	CLOCK	O
DDR2_CLK_P[1]	L20	CLOCK	O
DDR2_CLK_P[2]	H21	CLOCK	O
DDR2_CLK_P[3]	L22	CLOCK	O
DDR2_CS#[0]	G16	CMOS	O
DDR2_CS#[1]	K14	CMOS	O
DDR2_CS#[2]	D16	CMOS	O
DDR2_CS#[3]	H16	CMOS	O
DDR2_CS#[4]	E17	CMOS	O
DDR2_CS#[5]	D9	CMOS	O
DDR2_CS#[6]/ DDR2_ODT[4]	L17	CMOS	O
DDR2_CS#[7]/ DDR2_ODT[5]	J15	CMOS	O
DDR2_DQ[0]	W34	CMOS	I/O
DDR2_DQ[1]	W35	CMOS	I/O
DDR2_DQ[10]	R39	CMOS	I/O
DDR2_DQ[11]	T36	CMOS	I/O
DDR2_DQ[12]	W39	CMOS	I/O
DDR2_DQ[13]	V39	CMOS	I/O
DDR2_DQ[14]	T41	CMOS	I/O
DDR2_DQ[15]	R40	CMOS	I/O
DDR2_DQ[16]	M39	CMOS	I/O
DDR2_DQ[17]	M40	CMOS	I/O
DDR2_DQ[18]	J40	CMOS	I/O
DDR2_DQ[19]	J39	CMOS	I/O
DDR2_DQ[2]	V36	CMOS	I/O
DDR2_DQ[20]	P40	CMOS	I/O
DDR2_DQ[21]	N36	CMOS	I/O
DDR2_DQ[22]	L40	CMOS	I/O
DDR2_DQ[23]	K38	CMOS	I/O
DDR2_DQ[24]	G40	CMOS	I/O
DDR2_DQ[25]	F40	CMOS	I/O
DDR2_DQ[26]	J37	CMOS	I/O
DDR2_DQ[27]	H37	CMOS	I/O
DDR2_DQ[28]	H39	CMOS	I/O
DDR2_DQ[29]	G39	CMOS	I/O
DDR2_DQ[3]	U36	CMOS	I/O
DDR2_DQ[30]	F38	CMOS	I/O
DDR2_DQ[31]	E38	CMOS	I/O
DDR2_DQ[32]	K12	CMOS	I/O

Table 5-1. By Land Name (Sheet 15 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR2_DQ[33]	J12	CMOS	I/O
DDR2_DQ[34]	H13	CMOS	I/O
DDR2_DQ[35]	L13	CMOS	I/O
DDR2_DQ[36]	G11	CMOS	I/O
DDR2_DQ[37]	G10	CMOS	I/O
DDR2_DQ[38]	H12	CMOS	I/O
DDR2_DQ[39]	L12	CMOS	I/O
DDR2_DQ[4]	U34	CMOS	I/O
DDR2_DQ[40]	L10	CMOS	I/O
DDR2_DQ[41]	K10	CMOS	I/O
DDR2_DQ[42]	M9	CMOS	I/O
DDR2_DQ[43]	N9	CMOS	I/O
DDR2_DQ[44]	L11	CMOS	I/O
DDR2_DQ[45]	M10	CMOS	I/O
DDR2_DQ[46]	L8	CMOS	I/O
DDR2_DQ[47]	M8	CMOS	I/O
DDR2_DQ[48]	P7	CMOS	I/O
DDR2_DQ[49]	N6	CMOS	I/O
DDR2_DQ[5]	V34	CMOS	I/O
DDR2_DQ[50]	P9	CMOS	I/O
DDR2_DQ[51]	P10	CMOS	I/O
DDR2_DQ[52]	N8	CMOS	I/O
DDR2_DQ[53]	N7	CMOS	I/O
DDR2_DQ[54]	R10	CMOS	I/O
DDR2_DQ[55]	R9	CMOS	I/O
DDR2_DQ[56]	U5	CMOS	I/O
DDR2_DQ[57]	U6	CMOS	I/O
DDR2_DQ[58]	T10	CMOS	I/O
DDR2_DQ[59]	U10	CMOS	I/O
DDR2_DQ[6]	V37	CMOS	I/O
DDR2_DQ[60]	T6	CMOS	I/O
DDR2_DQ[61]	T7	CMOS	I/O
DDR2_DQ[62]	V8	CMOS	I/O
DDR2_DQ[63]	U9	CMOS	I/O
DDR2_DQ[7]	V38	CMOS	I/O
DDR2_DQ[8]	U38	CMOS	I/O
DDR2_DQ[9]	U39	CMOS	I/O
DDR2_DQS_N[0]	W36	CMOS	I/O
DDR2_DQS_N[1]	T38	CMOS	I/O
DDR2_DQS_N[10]	T40	CMOS	I/O
DDR2_DQS_N[11]	L38	CMOS	I/O

Table 5-1. By Land Name (Sheet 16 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR2_DQS_N[12]	G38	CMOS	I/O
DDR2_DQS_N[13]	J11	CMOS	I/O
DDR2_DQS_N[14]	K8	CMOS	I/O
DDR2_DQS_N[15]	P4	CMOS	I/O
DDR2_DQS_N[16]	V7	CMOS	I/O
DDR2_DQS_N[17]	G31	CMOS	I/O
DDR2_DQS_N[2]	K39	CMOS	I/O
DDR2_DQS_N[3]	E40	CMOS	I/O
DDR2_DQS_N[4]	J9	CMOS	I/O
DDR2_DQS_N[5]	K7	CMOS	I/O
DDR2_DQS_N[6]	P5	CMOS	I/O
DDR2_DQS_N[7]	T8	CMOS	I/O
DDR2_DQS_N[8]	G30	CMOS	I/O
DDR2_DQS_N[9]	T35	CMOS	I/O
DDR2_DQS_P[0]	W37	CMOS	I/O
DDR2_DQS_P[1]	T37	CMOS	I/O
DDR2_DQS_P[10]	U40	CMOS	I/O
DDR2_DQS_P[11]	M38	CMOS	I/O
DDR2_DQS_P[12]	H38	CMOS	I/O
DDR2_DQS_P[13]	H11	CMOS	I/O
DDR2_DQS_P[14]	K9	CMOS	I/O
DDR2_DQS_P[15]	N4	CMOS	I/O
DDR2_DQS_P[16]	V6	CMOS	I/O
DDR2_DQS_P[17]	H31	CMOS	I/O
DDR2_DQS_P[2]	K40	CMOS	I/O
DDR2_DQS_P[3]	E39	CMOS	I/O
DDR2_DQS_P[4]	J10	CMOS	I/O
DDR2_DQS_P[5]	L7	CMOS	I/O
DDR2_DQS_P[6]	P6	CMOS	I/O
DDR2_DQS_P[7]	U8	CMOS	I/O
DDR2_DQS_P[8]	G29	CMOS	I/O
DDR2_DQS_P[9]	U35	CMOS	I/O
DDR2_ECC[0]	H32	CMOS	I/O
DDR2_ECC[1]	F33	CMOS	I/O
DDR2_ECC[2]	E29	CMOS	I/O
DDR2_ECC[3]	E30	CMOS	I/O
DDR2_ECC[4]	J31	CMOS	I/O
DDR2_ECC[5]	J30	CMOS	I/O
DDR2_ECC[6]	F31	CMOS	I/O
DDR2_ECC[7]	F30	CMOS	I/O
DDR2_MA[0]	A18	CMOS	O

Table 5-1. By Land Name (Sheet 17 of 36)

Land Name	Land No.	Buffer Type	Direction
DDR2_MA[1]	K17	CMOS	O
DDR2_MA[10]	H17	CMOS	O
DDR2_MA[11]	H23	CMOS	O
DDR2_MA[12]	G23	CMOS	O
DDR2_MA[13]	F15	CMOS	O
DDR2_MA[14]	H24	CMOS	O
DDR2_MA[15]	G25	CMOS	O
DDR2_MA[2]	G18	CMOS	O
DDR2_MA[3]	J20	CMOS	O
DDR2_MA[4]	F20	CMOS	O
DDR2_MA[5]	K23	CMOS	O
DDR2_MA[6]	K22	CMOS	O
DDR2_MA[7]	J24	CMOS	O
DDR2_MA[8]	L25	CMOS	O
DDR2_MA[9]	H22	CMOS	O
DDR2_MA_PAR	B18	CMOS	O
DDR2_ODT[0]	L16	CMOS	O
DDR2_ODT[1]	F13	CMOS	O
DDR2_ODT[2]	D15	CMOS	O
DDR2_ODT[3]	D10	CMOS	O
DDR2_PAR_ERR#[0]	F21	Asynch	I
DDR2_PAR_ERR#[1]	J25	Asynch	I
DDR2_PAR_ERR#[2]	F23	Asynch	I
DDR2_RAS#	D17	CMOS	O
DDR2_RESET#	E32	CMOS	O
DDR2_WE#	C16	CMOS	O
GTLREF	AJ37	Analog	I
ISENSE	AK8	Analog	I
PECI	AH36	Asynch	I/O
PECI_ID#	AK35	Asynch	I
PRDY#	B41	GTL	O
PREQ#	C42	GTL	I
PROCHOT#	AG35	GTL	I/O
PSI#	AP7	CMOS	O
RESET#	AL39	Asynch	I
RSVD	A31		
RSVD	A40		
RSVD	AF1		
RSVD	AG1		
RSVD	AG4		
RSVD	AG5		

Table 5-1. By Land Name (Sheet 18 of 36)

Land Name	Land No.	Buffer Type	Direction
RSVD	AK2		
RSVD	AK7		
RSVD	AK36		
RSVD	AL3		
RSVD	AL38		
RSVD	AL4		
RSVD	AL40		
RSVD	AL41		
RSVD	AL5		
RSVD	AM36		
RSVD	AM38		
RSVD	AN36		
RSVD	AN38		
RSVD	AR36		
RSVD	AR37		
RSVD	AT36		
RSVD	AT4		
RSVD	AT5		
RSVD	AU2		
RSVD	AV1		
RSVD	AV2		
RSVD	AV35		
RSVD	AV42		
RSVD	AV43		
RSVD	AW2		
RSVD	AW39		
RSVD	AW41		
RSVD	AW42		
RSVD	AY3		
RSVD	AY35		
RSVD	AY39		
RSVD	AY4		
RSVD	AY40		
RSVD	AY41		
RSVD	B33		
RSVD	BA4		
RSVD	BA40		
RSVD	C31		
RSVD	C32		
RSVD	D30		
RSVD	D31		

Table 5-1. By Land Name (Sheet 19 of 36)

Land Name	Land No.	Buffer Type	Direction
RSVD	E28		
RSVD	F27		
RSVD	F28		
RSVD	G28		
RSVD	H29		
RSVD	J29		
RSVD	K15		
RSVD	K24		
RSVD	K25		
RSVD	K27		
RSVD	K29		
RSVD	L15		
RSVD	U11		
RSVD	V11		
SKTOCC#	AG36		O
TAPPWRGOOD	AH5	CMOS	O
TCK	AH10	TAP	I
TDI	AJ9	TAP	I
TDO	AJ10	TAP	O
THERMTRIP#	AG37	GTL	O
TMS	AG10	TAP	I
TRST#	AH9	TAP	I
VCC	AH11	PWR	
VCC	AH33	PWR	
VCC	AJ11	PWR	
VCC	AJ33	PWR	
VCC	AK11	PWR	
VCC	AK12	PWR	
VCC	AK13	PWR	
VCC	AK15	PWR	
VCC	AK16	PWR	
VCC	AK18	PWR	
VCC	AK19	PWR	
VCC	AK21	PWR	
VCC	AK24	PWR	
VCC	AK25	PWR	
VCC	AK27	PWR	
VCC	AK28	PWR	
VCC	AK30	PWR	
VCC	AK31	PWR	
VCC	AK33	PWR	

Table 5-1. By Land Name (Sheet 20 of 36)

Land Name	Land No.	Buffer Type	Direction
VCC	AL12	PWR	
VCC	AL13	PWR	
VCC	AL15	PWR	
VCC	AL16	PWR	
VCC	AL18	PWR	
VCC	AL19	PWR	
VCC	AL21	PWR	
VCC	AL24	PWR	
VCC	AL25	PWR	
VCC	AL27	PWR	
VCC	AL28	PWR	
VCC	AL30	PWR	
VCC	AL31	PWR	
VCC	AL33	PWR	
VCC	AL34	PWR	
VCC	AM12	PWR	
VCC	AM13	PWR	
VCC	AM15	PWR	
VCC	AM16	PWR	
VCC	AM18	PWR	
VCC	AM19	PWR	
VCC	AM21	PWR	
VCC	AM24	PWR	
VCC	AM25	PWR	
VCC	AM27	PWR	
VCC	AM28	PWR	
VCC	AM30	PWR	
VCC	AM31	PWR	
VCC	AM33	PWR	
VCC	AM34	PWR	
VCC	AN12	PWR	
VCC	AN13	PWR	
VCC	AN15	PWR	
VCC	AN16	PWR	
VCC	AN18	PWR	
VCC	AN19	PWR	
VCC	AN21	PWR	
VCC	AN24	PWR	
VCC	AN25	PWR	
VCC	AN27	PWR	
VCC	AN28	PWR	

Table 5-1. By Land Name (Sheet 21 of 36)

Land Name	Land No.	Buffer Type	Direction
VCC	AN30	PWR	
VCC	AN31	PWR	
VCC	AN33	PWR	
VCC	AN34	PWR	
VCC	AP12	PWR	
VCC	AP13	PWR	
VCC	AP15	PWR	
VCC	AP16	PWR	
VCC	AP18	PWR	
VCC	AP19	PWR	
VCC	AP21	PWR	
VCC	AP24	PWR	
VCC	AP25	PWR	
VCC	AP27	PWR	
VCC	AP28	PWR	
VCC	AP30	PWR	
VCC	AP31	PWR	
VCC	AP33	PWR	
VCC	AP34	PWR	
VCC	AR10	PWR	
VCC	AR12	PWR	
VCC	AR13	PWR	
VCC	AR15	PWR	
VCC	AR16	PWR	
VCC	AR18	PWR	
VCC	AR19	PWR	
VCC	AR21	PWR	
VCC	AR24	PWR	
VCC	AR25	PWR	
VCC	AR27	PWR	
VCC	AR28	PWR	
VCC	AR30	PWR	
VCC	AR31	PWR	
VCC	AR33	PWR	
VCC	AR34	PWR	
VCC	AT10	PWR	
VCC	AT12	PWR	
VCC	AT13	PWR	
VCC	AT15	PWR	
VCC	AT16	PWR	
VCC	AT18	PWR	

Table 5-1. By Land Name (Sheet 22 of 36)

Land Name	Land No.	Buffer Type	Direction
VCC	AT19	PWR	
VCC	AT21	PWR	
VCC	AT24	PWR	
VCC	AT25	PWR	
VCC	AT27	PWR	
VCC	AT28	PWR	
VCC	AT30	PWR	
VCC	AT31	PWR	
VCC	AT33	PWR	
VCC	AT34	PWR	
VCC	AT9	PWR	
VCC	AU10	PWR	
VCC	AU12	PWR	
VCC	AU13	PWR	
VCC	AU15	PWR	
VCC	AU16	PWR	
VCC	AU18	PWR	
VCC	AU19	PWR	
VCC	AU21	PWR	
VCC	AU24	PWR	
VCC	AU25	PWR	
VCC	AU27	PWR	
VCC	AU28	PWR	
VCC	AU30	PWR	
VCC	AU31	PWR	
VCC	AU33	PWR	
VCC	AU34	PWR	
VCC	AU9	PWR	
VCC	AV10	PWR	
VCC	AV12	PWR	
VCC	AV13	PWR	
VCC	AV15	PWR	
VCC	AV16	PWR	
VCC	AV18	PWR	
VCC	AV19	PWR	
VCC	AV21	PWR	
VCC	AV24	PWR	
VCC	AV25	PWR	
VCC	AV27	PWR	
VCC	AV28	PWR	
VCC	AV30	PWR	

Table 5-1. By Land Name (Sheet 23 of 36)

Land Name	Land No.	Buffer Type	Direction
VCC	AV31	PWR	
VCC	AV33	PWR	
VCC	AV34	PWR	
VCC	AV9	PWR	
VCC	AW10	PWR	
VCC	AW12	PWR	
VCC	AW13	PWR	
VCC	AW15	PWR	
VCC	AW16	PWR	
VCC	AW18	PWR	
VCC	AW19	PWR	
VCC	AW21	PWR	
VCC	AW24	PWR	
VCC	AW25	PWR	
VCC	AW27	PWR	
VCC	AW28	PWR	
VCC	AW30	PWR	
VCC	AW31	PWR	
VCC	AW33	PWR	
VCC	AW34	PWR	
VCC	AW9	PWR	
VCC	AY10	PWR	
VCC	AY12	PWR	
VCC	AY13	PWR	
VCC	AY15	PWR	
VCC	AY16	PWR	
VCC	AY18	PWR	
VCC	AY19	PWR	
VCC	AY21	PWR	
VCC	AY24	PWR	
VCC	AY25	PWR	
VCC	AY27	PWR	
VCC	AY28	PWR	
VCC	AY30	PWR	
VCC	AY31	PWR	
VCC	AY33	PWR	
VCC	AY34	PWR	
VCC	AY9	PWR	
VCC	BA10	PWR	
VCC	BA12	PWR	
VCC	BA13	PWR	

Table 5-1. By Land Name (Sheet 24 of 36)

Land Name	Land No.	Buffer Type	Direction
VCC	BA15	PWR	
VCC	BA16	PWR	
VCC	BA18	PWR	
VCC	BA19	PWR	
VCC	BA24	PWR	
VCC	BA25	PWR	
VCC	BA27	PWR	
VCC	BA28	PWR	
VCC	BA30	PWR	
VCC	BA9	PWR	
VCC	M11	PWR	
VCC	M13	PWR	
VCC	M15	PWR	
VCC	M19	PWR	
VCC	M21	PWR	
VCC	M23	PWR	
VCC	M25	PWR	
VCC	M29	PWR	
VCC	M31	PWR	
VCC	M33	PWR	
VCC	N11	PWR	
VCC	N33	PWR	
VCC	R11	PWR	
VCC	R33	PWR	
VCC	T11	PWR	
VCC	T33	PWR	
VCC	W11	PWR	
VCC_SENSE	AR9	Analog	
VCCPLL	U33	PWR	
VCCPLL	V33	PWR	
VCCPLL	W33	PWR	
VCCPWRGOOD	AR7	Asynch	I
VDDPWRGOOD	AA6	Asynch	I
VDDQ	A14	PWR	
VDDQ	A19	PWR	
VDDQ	A24	PWR	
VDDQ	A29	PWR	
VDDQ	A9	PWR	
VDDQ	B12	PWR	
VDDQ	B17	PWR	
VDDQ	B22	PWR	

Table 5-1. By Land Name (Sheet 25 of 36)

Land Name	Land No.	Buffer Type	Direction
VDDQ	B27	PWR	
VDDQ	B32	PWR	
VDDQ	B7	PWR	
VDDQ	C10	PWR	
VDDQ	C15	PWR	
VDDQ	C20	PWR	
VDDQ	C25	PWR	
VDDQ	C30	PWR	
VDDQ	D13	PWR	
VDDQ	D18	PWR	
VDDQ	D23	PWR	
VDDQ	D28	PWR	
VDDQ	E11	PWR	
VDDQ	E16	PWR	
VDDQ	E21	PWR	
VDDQ	E26	PWR	
VDDQ	E31	PWR	
VDDQ	F14	PWR	
VDDQ	F19	PWR	
VDDQ	F24	PWR	
VDDQ	G17	PWR	
VDDQ	G22	PWR	
VDDQ	G27	PWR	
VDDQ	H15	PWR	
VDDQ	H20	PWR	
VDDQ	H25	PWR	
VDDQ	J18	PWR	
VDDQ	J23	PWR	
VDDQ	J28	PWR	
VDDQ	K16	PWR	
VDDQ	K21	PWR	
VDDQ	K26	PWR	
VDDQ	L14	PWR	
VDDQ	L19	PWR	
VDDQ	L24	PWR	
VDDQ	M17	PWR	
VDDQ	M27	PWR	
VID[0]/MSID[0]	AL10	CMOS	O
VID[1]/MSID[1]	AL9	CMOS	O
VID[2]/MSID[2]	AN9	CMOS	O
VID[3]/CSC[0]	AM10	CMOS	O

Table 5-1. By Land Name (Sheet 26 of 36)

Land Name	Land No.	Buffer Type	Direction
VID[4]/CSC[1]	AN10	CMOS	O
VID[5]/CSC[2]	AP9	CSMO	O
VID[6]	AP8	CMOS	O
VID[7]	AN8	CMOS	O
VSS	A35	GND	
VSS	A39	GND	
VSS	A4	GND	
VSS	A41	GND	
VSS	A6	GND	
VSS	AA3	GND	
VSS	AA34	GND	
VSS	AA38	GND	
VSS	AA39	GND	
VSS	AA9	GND	
VSS	AB37	GND	
VSS	AB4	GND	
VSS	AB40	GND	
VSS	AB42	GND	
VSS	AB7	GND	
VSS	AC2	GND	
VSS	AC36	GND	
VSS	AC5	GND	
VSS	AC7	GND	
VSS	AC9	GND	
VSS	AD11	GND	
VSS	AD33	GND	
VSS	AD37	GND	
VSS	AD41	GND	
VSS	AD43	GND	
VSS	AE2	GND	
VSS	AE39	GND	
VSS	AE7	GND	
VSS	AF35	GND	
VSS	AF38	GND	
VSS	AF41	GND	
VSS	AF5	GND	
VSS	AG11	GND	
VSS	AG3	GND	
VSS	AG33	GND	
VSS	AG43	GND	
VSS	AG9	GND	

Table 5-1. By Land Name (Sheet 27 of 36)

Land Name	Land No.	Buffer Type	Direction
VSS	AH1	GND	
VSS	AH34	GND	
VSS	AH37	GND	
VSS	AH39	GND	
VSS	AH7	GND	
VSS	AJ34	GND	
VSS	AJ36	GND	
VSS	AJ41	GND	
VSS	AJ5	GND	
VSS	AK10	GND	
VSS	AK14	GND	
VSS	AK17	GND	
VSS	AK20	GND	
VSS	AK22	GND	
VSS	AK23	GND	
VSS	AK26	GND	
VSS	AK29	GND	
VSS	AK3	GND	
VSS	AK32	GND	
VSS	AK34	GND	
VSS	AK39	GND	
VSS	AK43	GND	
VSS	AK9	GND	
VSS	AL1	GND	
VSS	AL11	GND	
VSS	AL14	GND	
VSS	AL17	GND	
VSS	AL2	GND	
VSS	AL20	GND	
VSS	AL22	GND	
VSS	AL23	GND	
VSS	AL26	GND	
VSS	AL29	GND	
VSS	AL32	GND	
VSS	AL35	GND	
VSS	AL36	GND	
VSS	AL37	GND	
VSS	AL42	GND	
VSS	AL7	GND	
VSS	AM11	GND	
VSS	AM14	GND	

Table 5-1. By Land Name (Sheet 28 of 36)

Land Name	Land No.	Buffer Type	Direction
VSS	AM17	GND	
VSS	AM20	GND	
VSS	AM22	GND	
VSS	AM23	GND	
VSS	AM26	GND	
VSS	AM29	GND	
VSS	AM32	GND	
VSS	AM35	GND	
VSS	AM37	GND	
VSS	AM39	GND	
VSS	AM5	GND	
VSS	AM9	GND	
VSS	AN11	GND	
VSS	AN14	GND	
VSS	AN17	GND	
VSS	AN20	GND	
VSS	AN22	GND	
VSS	AN23	GND	
VSS	AN26	GND	
VSS	AN29	GND	
VSS	AN3	GND	
VSS	AN32	GND	
VSS	AN35	GND	
VSS	AN37	GND	
VSS	AN41	GND	
VSS	AN7	GND	
VSS	AP1	GND	
VSS	AP10	GND	
VSS	AP11	GND	
VSS	AP14	GND	
VSS	AP17	GND	
VSS	AP20	GND	
VSS	AP22	GND	
VSS	AP23	GND	
VSS	AP26	GND	
VSS	AP29	GND	
VSS	AP32	GND	
VSS	AP35	GND	
VSS	AP36	GND	
VSS	AP37	GND	
VSS	AP43	GND	

Table 5-1. By Land Name (Sheet 29 of 36)

Land Name	Land No.	Buffer Type	Direction
VSS	AP5	GND	
VSS	AP6	GND	
VSS	AR11	GND	
VSS	AR14	GND	
VSS	AR17	GND	
VSS	AR2	GND	
VSS	AR20	GND	
VSS	AR22	GND	
VSS	AR23	GND	
VSS	AR26	GND	
VSS	AR29	GND	
VSS	AR3	GND	
VSS	AR32	GND	
VSS	AR35	GND	
VSS	AR39	GND	
VSS	AT11	GND	
VSS	AT14	GND	
VSS	AT17	GND	
VSS	AT20	GND	
VSS	AT22	GND	
VSS	AT23	GND	
VSS	AT26	GND	
VSS	AT29	GND	
VSS	AT32	GND	
VSS	AT35	GND	
VSS	AT38	GND	
VSS	AT41	GND	
VSS	AT7	GND	
VSS	AT8	GND	
VSS	AU1	GND	
VSS	AU11	GND	
VSS	AU14	GND	
VSS	AU17	GND	
VSS	AU20	GND	
VSS	AU22	GND	
VSS	AU23	GND	
VSS	AU26	GND	
VSS	AU29	GND	
VSS	AU32	GND	
VSS	AU35	GND	
VSS	AU36	GND	

Table 5-1. By Land Name (Sheet 30 of 36)

Land Name	Land No.	Buffer Type	Direction
VSS	AU43	GND	
VSS	AU5	GND	
VSS	AV11	GND	
VSS	AV14	GND	
VSS	AV17	GND	
VSS	AV20	GND	
VSS	AV22	GND	
VSS	AV23	GND	
VSS	AV26	GND	
VSS	AV29	GND	
VSS	AV32	GND	
VSS	AV39	GND	
VSS	AV4	GND	
VSS	AV41	GND	
VSS	AW1	GND	
VSS	AW11	GND	
VSS	AW14	GND	
VSS	AW17	GND	
VSS	AW20	GND	
VSS	AW22	GND	
VSS	AW23	GND	
VSS	AW26	GND	
VSS	AW29	GND	
VSS	AW32	GND	
VSS	AW35	GND	
VSS	AW6	GND	
VSS	AW8	GND	
VSS	AY11	GND	
VSS	AY14	GND	
VSS	AY17	GND	
VSS	AY2	GND	
VSS	AY20	GND	
VSS	AY22	GND	
VSS	AY23	GND	
VSS	AY26	GND	
VSS	AY29	GND	
VSS	AY32	GND	
VSS	AY37	GND	
VSS	AY42	GND	
VSS	AY7	GND	
VSS	B2	GND	

Table 5-1. By Land Name (Sheet 31 of 36)

Land Name	Land No.	Buffer Type	Direction
VSS	B37	GND	
VSS	B42	GND	
VSS	BA11	GND	
VSS	BA14	GND	
VSS	BA17	GND	
VSS	BA20	GND	
VSS	BA26	GND	
VSS	BA29	GND	
VSS	BA3	GND	
VSS	BA35	GND	
VSS	BA39	GND	
VSS	BA5	GND	
VSS	C35	GND	
VSS	C40	GND	
VSS	C43	GND	
VSS	C5	GND	
VSS	D3	GND	
VSS	D33	GND	
VSS	D38	GND	
VSS	D43	GND	
VSS	D8	GND	
VSS	E1	GND	
VSS	E36	GND	
VSS	E41	GND	
VSS	E6	GND	
VSS	F29	GND	
VSS	F34	GND	
VSS	F39	GND	
VSS	F4	GND	
VSS	F9	GND	
VSS	G12	GND	
VSS	G2	GND	
VSS	G32	GND	
VSS	G37	GND	
VSS	G42	GND	
VSS	G7	GND	
VSS	H10	GND	
VSS	H30	GND	
VSS	H35	GND	
VSS	H40	GND	
VSS	H5	GND	

Table 5-1. By Land Name (Sheet 32 of 36)

Land Name	Land No.	Buffer Type	Direction
VSS	J13	GND	
VSS	J3	GND	
VSS	J33	GND	
VSS	J38	GND	
VSS	J43	GND	
VSS	J8	GND	
VSS	K1	GND	
VSS	K11	GND	
VSS	K31	GND	
VSS	K36	GND	
VSS	K41	GND	
VSS	K6	GND	
VSS	L29	GND	
VSS	L34	GND	
VSS	L39	GND	
VSS	L4	GND	
VSS	L9	GND	
VSS	M12	GND	
VSS	M14	GND	
VSS	M16	GND	
VSS	M18	GND	
VSS	M2	GND	
VSS	M20	GND	
VSS	M22	GND	
VSS	M24	GND	
VSS	M26	GND	
VSS	M28	GND	
VSS	M30	GND	
VSS	M32	GND	
VSS	M37	GND	
VSS	M42	GND	
VSS	M7	GND	
VSS	N10	GND	
VSS	N35	GND	
VSS	N40	GND	
VSS	N5	GND	
VSS	P11	GND	
VSS	P3	GND	
VSS	P33	GND	
VSS	P38	GND	
VSS	P43	GND	

Table 5-1. By Land Name (Sheet 33 of 36)

Land Name	Land No.	Buffer Type	Direction
VSS	P8	GND	
VSS	R1	GND	
VSS	R36	GND	
VSS	R41	GND	
VSS	R6	GND	
VSS	T34	GND	
VSS	T39	GND	
VSS	T4	GND	
VSS	T9	GND	
VSS	U2	GND	
VSS	U37	GND	
VSS	U42	GND	
VSS	U7	GND	
VSS	V10	GND	
VSS	V35	GND	
VSS	V40	GND	
VSS	V5	GND	
VSS	W3	GND	
VSS	W38	GND	
VSS	W43	GND	
VSS	W8	GND	
VSS	Y1	GND	
VSS	Y11	GND	
VSS	Y33	GND	
VSS	Y36	GND	
VSS	Y41	GND	
VSS	Y6	GND	
VSS_SENSE	AR8	Analog	
VSS_SENSE_VTTD	AE37	Analog	
VTT_VID2	AV3	CMOS	O
VTT_VID3	AF7	CMOS	O
VTT_VID4	AV6	CMOS	O
VTTA	AD10	PWR	
VTTA	AE10	PWR	
VTTA	AE11	PWR	
VTTA	AE33	PWR	
VTTA	AF11	PWR	
VTTA	AF33	PWR	
VTTA	AF34	PWR	
VTTA	AG34	PWR	
VTTD	AA10	PWR	

Table 5-1. By Land Name (Sheet 34 of 36)

Land Name	Land No.	Buffer Type	Direction
VTTD	AA11	PWR	
VTTD	AA33	PWR	
VTTD	AB10	PWR	
VTTD	AB11	PWR	
VTTD	AB33	PWR	
VTTD	AB34	PWR	
VTTD	AB8	PWR	
VTTD	AB9	PWR	
VTTD	AC10	PWR	
VTTD	AC11	PWR	
VTTD	AC33	PWR	
VTTD	AC34	PWR	
VTTD	AC35	PWR	

Table 5-1. By Land Name (Sheet 35 of 36)

Land Name	Land No.	Buffer Type	Direction
VTTD	AD34	PWR	
VTTD	AD35	PWR	
VTTD	AD36	PWR	
VTTD	AD9	PWR	
VTTD	AE34	PWR	
VTTD	AE35	PWR	
VTTD	AE8	PWR	

Table 5-1. By Land Name (Sheet 36 of 36)

Land Name	Land No.	Buffer Type	Direction
VTTD	AE9	PWR	
VTTD	AF36	PWR	
VTTD	AF37	PWR	
VTTD	AF8	PWR	
VTTD	AF9	PWR	
VTTD_SENSE	AE36	Analog	
VTTPWRGOOD	AB35	Asynch	I

5.2 Listing by Land Number

Table 5-2. By Land Number (Sheet 1 of 35)

Land Name	Land No.	Buffer Type	Direction
DDR0_MA[13]	A10	CMOS	O
VDDQ	A14	PWR	
DDR0_RAS#	A15	CMOS	O
DDR0_BA[1]	A16	CMOS	O
DDR2_BA[0]	A17	CMOS	O
DDR2_MA[0]	A18	CMOS	O
VDDQ	A19	PWR	
DDR0_MA[0]	A20	CMOS	O
VDDQ	A24	PWR	
DDR0_MA[7]	A25	CMOS	O
DDR0_MA[11]	A26	CMOS	O
DDR0_PAR_ERR#[2]	A27	Asynch	I
DDR0_MA[14]	A28	CMOS	O
VDDQ	A29	PWR	
DDR0_CKE[1]	A30	CMOS	O
RSVD	A31		
VSS	A35	GND	
DDR0_ECC[1]	A36	CMOS	I/O
DDR0_ECC[5]	A37	CMOS	I/O
DDR0_DQ[26]	A38	CMOS	I/O
VSS	A39	GND	
VSS	A4	GND	
RSVD	A40		
VSS	A41	GND	
BPM#[1]	A5	GTL	I/O
VSS	A6	GND	
DDR0_CS#[5]	A7	CMOS	O
DDR1_CS#[1]	A8	CMOS	O

Table 5-2. By Land Number (Sheet 2 of 35)

Land Name	Land No.	Buffer Type	Direction
VDDQ	A9	PWR	
VTTD	AA10	PWR	
VTTD	AA11	PWR	
VSS	AA3	GND	
VTTD	AA33	PWR	
VSS	AA34	GND	
DDR1_DQ[4]	AA35	CMOS	I/O
DDR1_DQ[1]	AA36	CMOS	I/O
DDR1_DQ[0]	AA37	CMOS	I/O
VSS	AA38	GND	
VSS	AA39	GND	
BCLK_ITP_DN	AA4	CMOS	O
DDR1_DQS_P[9]	AA40	CMOS	I/O
DDR1_DQS_N[9]	AA41	CMOS	I/O
BCLK_ITP_DP	AA5	CMOS	O
VDDPWRGOOD	AA6	Asynch	I
DDR1_DQ[62]	AA7	CMOS	I/O
DDR_COMP[0]	AA8	Analog	
VSS	AA9	GND	
VTTD	AB10	PWR	
VTTD	AB11	PWR	
QPI1_DTX_DN[13]	AB3	QPI	O
VTTD	AB33	PWR	
VTTD	AB34	PWR	
VTTPWRGOOD	AB35	Asynch	I
DDR1_DQ[5]	AB36	CMOS	I/O
VSS	AB37	GND	
QPI0_DTX_DN[17]	AB38	QPI	O

Table 5-2. By Land Number (Sheet 3 of 35)

Land Name	Land No.	Buffer Type	Direction
QPI0_DTX_DP[17]	AB39	QPI	O
VSS	AB4	GND	
VSS	AB40	GND	
COMP0	AB41	Analog	
VSS	AB42	GND	
QPI0_DTX_DN[13]	AB43	QPI	O
DDR_THERM#	AB5	CMOS	I
QPI1_DTX_DP[16]	AB6	QPI	O
VSS	AB7	GND	
VTTD	AB8	PWR	
VTTD	AB9	PWR	
DDR_COMP[2]	AC1	Analog	
VTTD	AC10	PWR	
VTTD	AC11	PWR	
VSS	AC2	GND	
QPI1_DTX_DP[13]	AC3	QPI	O
VTTD	AC33	PWR	
VTTD	AC34	PWR	
VTTD	AC35	PWR	
VSS	AC36	GND	
CAT_ERR#	AC37	GTL	I/O
QPI0_DTX_DN[16]	AC38	QPI	O
QPI0_DTX_DP[16]	AC39	QPI	O
QPI1_DTX_DP[15]	AC4	QPI	O
QPI0_DTX_DN[15]	AC40	QPI	O
QPI0_DTX_DP[15]	AC41	QPI	O
QPI0_DTX_DN[12]	AC42	QPI	O
QPI0_DTX_DP[13]	AC43	QPI	O
VSS	AC5	GND	
QPI1_DTX_DN[16]	AC6	QPI	O
VSS	AC7	GND	
QPI1_DTX_DP[19]	AC8	QPI	O
VSS	AC9	GND	
QPI1_DTX_DN[11]	AD1	QPI	O
VTTA	AD10	PWR	
VSS	AD11	GND	
QPI1_DTX_DP[12]	AD2	QPI	O
QPI1_DTX_DN[12]	AD3	QPI	O
VSS	AD33	GND	
VTTD	AD34	PWR	
VTTD	AD35	PWR	

Table 5-2. By Land Number (Sheet 4 of 35)

Land Name	Land No.	Buffer Type	Direction
VTTD	AD36	PWR	
VSS	AD37	GND	
QPI0_DTX_DP[18]	AD38	QPI	O
QPI0_DTX_DN[14]	AD39	QPI	O
QPI1_DTX_DN[15]	AD4	QPI	O
QPI0_DTX_DP[14]	AD40	QPI	O
VSS	AD41	GND	
QPI0_DTX_DP[12]	AD42	QPI	O
VSS	AD43	GND	
QPI1_DTX_DP[18]	AD5	QPI	O
QPI1_DTX_DP[17]	AD6	QPI	O
QPI1_DTX_DN[17]	AD7	QPI	O
QPI1_DTX_DN[19]	AD8	QPI	O
VTTD	AD9	PWR	
QPI1_DTX_DP[11]	AE1	QPI	O
VTTA	AE10	PWR	
VTTA	AE11	PWR	
VSS	AE2	GND	
QPI1_DTX_DP[14]	AE3	QPI	O
VTTA	AE33	PWR	
VTTD	AE34	PWR	
VTTD	AE35	PWR	
VTTD_SENSE	AE36	Analog	
VSS_SENSE_VTTD	AE37	Analog	
QPI0_DTX_DN[18]	AE38	QPI	O
VSS	AE39	GND	
QPI1_DTX_DN[14]	AE4	QPI	O
QPI0_DTX_DP[19]	AE40	QPI	O
QPI0_DTX_DN[11]	AE41	QPI	O
QPI0_DTX_DP[11]	AE42	QPI	O
QPI0_DTX_DN[10]	AE43	QPI	O
QPI1_DTX_DN[18]	AE5	QPI	O
QPI1_CLKTX_DN	AE6	QPI	O
VSS	AE7	GND	
VTTD	AE8	PWR	
VTTD	AE9	PWR	
RSVD	AF1		
DBR#	AF10	Asynch	I
VTTA	AF11	PWR	
QPI1_DTX_DP[10]	AF2	QPI	O
QPI1_DTX_DN[10]	AF3	QPI	O

Table 5-2. By Land Number (Sheet 5 of 35)

Land Name	Land No.	Buffer Type	Direction
VTTA	AF33	PWR	
VTTA	AF34	PWR	
VSS	AF35	GND	
VTTD	AF36	PWR	
VTTD	AF37		
VSS	AF38	GND	
QPI0_DTX_DP[1]	AF39	QPI	O
DDR_THERM2#	AF4		
QPI0_DTX_DN[19]	AF40	QPI	O
VSS	AF41	GND	
QPI0_CLKTX_DN	AF42	QPI	O
QPI0_DTX_DP[10]	AF43	QPI	O
VSS	AF5	GND	
QPI1_CLKTX_DP	AF6	QPI	O
VTT_VID3	AF7	CMOS	O
VTTD	AF8	PWR	
VTTD	AF9	PWR	
RSVD	AG1		
TMS	AG10	TAP	I
VSS	AG11	GND	
QPI1_DTX_DN[9]	AG2	QPI	O
VSS	AG3	GND	
VSS	AG33	GND	
VTTA	AG34	PWR	
PROCHOT#	AG35	GTL	I/O
SKTOCC#	AG36		O
THERMTRIP#	AG37	GTL	O
QPI0_DTX_DP[0]	AG38	QPI	O
QPI0_DTX_DN[1]	AG39	QPI	O
RSVD	AG4		
QPI0_DTX_DP[9]	AG40	QPI	O
QPI0_DTX_DN[9]	AG41	QPI	O
QPI0_CLKTX_DP	AG42	QPI	O
VSS	AG43	GND	
RSVD	AG5		
QPI1_DTX_DN[5]	AG6	QPI	O
QPI1_DTX_DP[5]	AG7	QPI	O
QPI1_DTX_DP[0]	AG8	QPI	O
VSS	AG9	GND	
VSS	AH1	GND	
TCK	AH10	TAP	I

Table 5-2. By Land Number (Sheet 6 of 35)

Land Name	Land No.	Buffer Type	Direction
VCC	AH11	PWR	
QPI1_DTX_DP[9]	AH2	QPI	O
QPI1_DTX_DP[8]	AH3	QPI	O
VCC	AH33	PWR	
VSS	AH34	GND	
BCLK_DN	AH35	CMOS	I
PECI	AH36	Asynch	I/O
VSS	AH37	GND	
QPI0_DTX_DN[0]	AH38	QPI	O
VSS	AH39	GND	
QPI1_DTX_DN[8]	AH4	QPI	O
QPI0_DTX_DP[4]	AH40	QPI	O
QPI0_DTX_DP[6]	AH41	QPI	O
QPI0_DTX_DN[6]	AH42	QPI	O
QPI0_DTX_DN[8]	AH43	QPI	O
TAPPWRGOOD	AH5		
QPI1_DTX_DP[2]	AH6	QPI	O
VSS	AH7	GND	
QPI1_DTX_DN[0]	AH8	QPI	O
TRST#	AH9	TAP	I
QPI1_DTX_DN[7]	AJ1	QPI	O
TDO	AJ10	TAP	O
VCC	AJ11	PWR	
QPI1_DTX_DN[6]	AJ2	QPI	O
QPI1_DTX_DP[6]	AJ3	QPI	O
VCC	AJ33	PWR	
VSS	AJ34	GND	
BCLK_DP	AJ35	CMOS	I
VSS	AJ36	GND	
GTLREF	AJ37	Analog	I
QPI0_DTX_DP[3]	AJ38	QPI	O
QPI0_DTX_DN[3]	AJ39	QPI	O
QPI1_DTX_DP[4]	AJ4	QPI	O
QPI0_DTX_DN[4]	AJ40	QPI	O
VSS	AJ41	GND	
QPI0_DTX_DN[7]	AJ42	QPI	O
QPI0_DTX_DP[8]	AJ43	QPI	O
VSS	AJ5	GND	
QPI1_DTX_DN[2]	AJ6	QPI	O
QPI1_DTX_DN[1]	AJ7	QPI	O
QPI1_DTX_DP[1]	AJ8	QPI	O

Table 5-2. By Land Number (Sheet 7 of 35)

Land Name	Land No.	Buffer Type	Direction
TDI	AJ9	TAP	I
QPI1_DTX_DP[7]	AK1	QPI	O
VSS	AK10	GND	
VCC	AK11	PWR	
VCC	AK12	PWR	
VCC	AK13	PWR	
VSS	AK14	GND	
VCC	AK15	PWR	
VCC	AK16	PWR	
VSS	AK17	GND	
VCC	AK18	PWR	
VCC	AK19	PWR	
RSVD	AK2		
VSS	AK20	GND	
VCC	AK21	PWR	
VSS	AK22	GND	
VSS	AK23	GND	
VCC	AK24	PWR	
VCC	AK25	PWR	
VSS	AK26	GND	
VCC	AK27	PWR	
VCC	AK28	PWR	
VSS	AK29	GND	
VSS	AK3	GND	
VCC	AK30	PWR	
VCC	AK31	PWR	
VSS	AK32	GND	
VCC	AK33	PWR	
VSS	AK34	GND	
PECI_ID#	AK35	Asynch	I
RSVD	AK36		
QPI0_DTX_DP[2]	AK37	QPI	O
QPI0_DTX_DN[2]	AK38	QPI	O
VSS	AK39	GND	
QPI1_DTX_DN[4]	AK4	QPI	O
QPI0_DTX_DP[5]	AK40	QPI	O
QPI0_DTX_DN[5]	AK41	QPI	O
QPI0_DTX_DP[7]	AK42	QPI	O
VSS	AK43	GND	
QPI1_DTX_DN[3]	AK5	QPI	O
QPI1_DTX_DP[3]	AK6	QPI	O

Table 5-2. By Land Number (Sheet 8 of 35)

Land Name	Land No.	Buffer Type	Direction
RSVD	AK7		
ISENSE	AK8	Analog	I
VSS	AK9	GND	
VSS	AL1	GND	
VID[0]/MSID[0]	AL10	CMOS	O
VSS	AL11	GND	
VCC	AL12	PWR	
VCC	AL13	PWR	
VSS	AL14	GND	
VCC	AL15	PWR	
VCC	AL16	PWR	
VSS	AL17	GND	
VCC	AL18	PWR	
VCC	AL19	PWR	
VSS	AL2	GND	
VSS	AL20	GND	
VCC	AL21	PWR	
VSS	AL22	GND	
VSS	AL23	GND	
VCC	AL24	PWR	
VCC	AL25	PWR	
VSS	AL26	GND	
VCC	AL27	PWR	
VCC	AL28	PWR	
VSS	AL29	GND	
RSVD	AL3		
VCC	AL30	PWR	
VCC	AL31	PWR	
VSS	AL32	GND	
VCC	AL33	PWR	
VCC	AL34	PWR	
VSS	AL35	GND	
VSS	AL36	GND	
VSS	AL37	GND	
RSVD	AL38		
RESET#	AL39	Asynch	I
RSVD	AL4		
RSVD	AL40		
RSVD	AL41		
VSS	AL42	GND	
QPI0_COMP	AL43	Analog	

Table 5-2. By Land Number (Sheet 9 of 35)

Land Name	Land No.	Buffer Type	Direction
RSVD	AL5		
QPI1_COMP	AL6	Analog	
VSS	AL7	GND	
QPI1_DRX_DN[19]	AL8	QPI	I
VID[1]/MSID[1]	AL9	CMOS	O
QPI1_DRX_DN[13]	AM1	QPI	I
VID[3]/CSC[0]	AM10	CMOS	O
VSS	AM11	GND	
VCC	AM12	PWR	
VCC	AM13	PWR	
VSS	AM14	GND	
VCC	AM15	PWR	
VCC	AM16	PWR	
VSS	AM17	GND	
VCC	AM18	PWR	
VCC	AM19	PWR	
QPI1_DRX_DP[14]	AM2	QPI	I
VSS	AM20	GND	
VCC	AM21	PWR	
VSS	AM22	GND	
VSS	AM23	GND	
VCC	AM24	PWR	
VCC	AM25	PWR	
VSS	AM26	GND	
VCC	AM27	PWR	
VCC	AM28	PWR	
VSS	AM29	GND	
QPI1_DRX_DN[14]	AM3	QPI	I
VCC	AM30	PWR	
VCC	AM31	PWR	
VSS	AM32	GND	
VCC	AM33	PWR	
VCC	AM34	PWR	
VSS	AM35	GND	
RSVD	AM36		
VSS	AM37	GND	
RSVD	AM38		
VSS	AM39	GND	
QPI1_DRX_DP[16]	AM4	QPI	I
QPI0_DRX_DN[15]	AM40	QPI	I
QPI0_DRX_DN[16]	AM41	QPI	I

Table 5-2. By Land Number (Sheet 10 of

Land Name	Land No.	Buffer Type	Direction
QPI0_DRX_DP[16]	AM42	QPI	I
QPI0_DRX_DN[14]	AM43	QPI	I
VSS	AM5	GND	
QPI1_DRX_DP[18]	AM6	QPI	I
QPI1_DRX_DN[18]	AM7	QPI	I
QPI1_DRX_DP[19]	AM8	QPI	I
VSS	AM9	GND	
QPI1_DRX_DP[13]	AN1	QPI	I
VID[4]/CSC[1]	AN10	CMOS	O
VSS	AN11	GND	
VCC	AN12	PWR	
VCC	AN13	PWR	
VSS	AN14	GND	
VCC	AN15	PWR	
VCC	AN16	PWR	
VSS	AN17	GND	
VCC	AN18	PWR	
VCC	AN19	PWR	
QPI1_DRX_DN[12]	AN2	QPI	I
VSS	AN20	GND	
VCC	AN21	PWR	
VSS	AN22	GND	
VSS	AN23	GND	
VCC	AN24	PWR	
VCC	AN25	PWR	
VSS	AN26	GND	
VCC	AN27	PWR	
VCC	AN28	PWR	
VSS	AN29	GND	
VSS	AN3	GND	
VCC	AN30	PWR	
VCC	AN31	PWR	
VSS	AN32	GND	
VCC	AN33	PWR	
VCC	AN34	PWR	
VSS	AN35	GND	
RSVD	AN36		
VSS	AN37	GND	
RSVD	AN38		
QPI0_DRX_DP[18]	AN39	QPI	I
QPI1_DRX_DN[16]	AN4	QPI	I

Table 5-2. By Land Number (Sheet 11 of

Land Name	Land No.	Buffer Type	Direction
QPI0_DRX_DP[15]	AN40	QPI	I
VSS	AN41	GND	
QPI0_DRX_DN[13]	AN42	QPI	I
QPI0_DRX_DP[14]	AN43	QPI	I
QPI1_DRX_DP[17]	AN5	QPI	I
QPI1_DRX_DN[17]	AN6	QPI	I
VSS	AN7	GND	
VID[7]	AN8	CMOS	O
VID[2]/MSID[2]	AN9	CMOS	O
VSS	AP1	GND	
VSS	AP10	GND	
VSS	AP11	GND	
VCC	AP12	PWR	
VCC	AP13	PWR	
VSS	AP14	GND	
VCC	AP15	PWR	
VCC	AP16	PWR	
VSS	AP17	GND	
VCC	AP18	PWR	
VCC	AP19	PWR	
QPI1_DRX_DP[12]	AP2	QPI	I
VSS	AP20	GND	
VCC	AP21	PWR	
VSS	AP22	GND	
VSS	AP23	GND	
VCC	AP24	PWR	
VCC	AP25	PWR	
VSS	AP26	GND	
VCC	AP27	PWR	
VCC	AP28	PWR	
VSS	AP29	GND	
QPI1_DRX_DP[15]	AP3	QPI	I
VCC	AP30	PWR	
VCC	AP31	PWR	
VSS	AP32	GND	
VCC	AP33	PWR	
VCC	AP34	PWR	
VSS	AP35	GND	
VSS	AP36	GND	
VSS	AP37	GND	
QPI0_DRX_DP[19]	AP38	QPI	I

Table 5-2. By Land Number (Sheet 12 of

Land Name	Land No.	Buffer Type	Direction
QPI0_DRX_DN[18]	AP39	QPI	I
QPI1_DRX_DN[15]	AP4	QPI	I
QPI0_DRX_DN[17]	AP40	QPI	I
QPI0_DRX_DP[17]	AP41	QPI	I
QPI0_DRX_DP[13]	AP42	QPI	I
VSS	AP43	GND	
VSS	AP5	GND	
VSS	AP6	GND	
PSI#	AP7	CMOS	O
VID[6]	AP8	CMOS	O
VID[5]/CSC[2]	AP9	CMOS	O
QPI1_DRX_DN[10]	AR1	QPI	I
VCC	AR10	PWR	
VSS	AR11	GND	
VCC	AR12	PWR	
VCC	AR13	PWR	
VSS	AR14	GND	
VCC	AR15	PWR	
VCC	AR16	PWR	
VSS	AR17	GND	
VCC	AR18	PWR	
VCC	AR19	PWR	
VSS	AR2	GND	
VSS	AR20	GND	
VCC	AR21	PWR	
VSS	AR22	GND	
VSS	AR23	GND	
VCC	AR24	PWR	
VCC	AR25	PWR	
VSS	AR26	GND	
VCC	AR27	PWR	
VCC	AR28	PWR	
VSS	AR29	GND	
VSS	AR3	GND	
VCC	AR30	PWR	
VCC	AR31	PWR	
VSS	AR32	GND	
VCC	AR33	PWR	
VCC	AR34	PWR	
VSS	AR35	GND	
RSVD	AR36		

Table 5-2. By Land Number (Sheet 13 of

Land Name	Land No.	Buffer Type	Direction
RSVD	AR37		
QPI0_DRX_DN[19]	AR38	QPI	I
VSS	AR39	GND	
QPI1_DRX_DP[11]	AR4	QPI	I
QPI0_DRX_DN[12]	AR40	QPI	I
QPI0_CLKRX_DP	AR41	QPI	I
QPI0_CLKRX_DN	AR42	QPI	I
QPI0_DRX_DN[11]	AR43	QPI	I
QPI1_DRX_DN[11]	AR5	QPI	I
QPI1_CLKRX_DN	AR6	QPI	I
VCCPWRGOOD	AR7	Asynch	I
VSS_SENSE	AR8	Analog	
VCC_SENSE	AR9	Analog	
QPI1_DRX_DP[10]	AT1	QPI	I
VCC	AT10	PWR	
VSS	AT11	GND	
VCC	AT12	PWR	
VCC	AT13	PWR	
VSS	AT14	GND	
VCC	AT15	PWR	
VCC	AT16	PWR	
VSS	AT17	GND	
VCC	AT18	PWR	
VCC	AT19	PWR	
QPI1_DRX_DN[9]	AT2	QPI	I
VSS	AT20	GND	
VCC	AT21	PWR	
VSS	AT22	GND	
VSS	AT23	GND	
VCC	AT24	PWR	
VCC	AT25	PWR	
VSS	AT26	GND	
VCC	AT27	PWR	
VCC	AT28	PWR	
VSS	AT29	GND	
QPI1_DRX_DP[9]	AT3	QPI	I
VCC	AT30	PWR	
VCC	AT31	PWR	
VSS	AT32	GND	
VCC	AT33	PWR	
VCC	AT34	PWR	

Table 5-2. By Land Number (Sheet 14 of

Land Name	Land No.	Buffer Type	Direction
VSS	AT35	GND	
RSVD	AT36		
QPI0_DRX_DP[0]	AT37	QPI	I
VSS	AT38	GND	
QPI0_DRX_DN[7]	AT39	QPI	I
RSVD	AT4		
QPI0_DRX_DP[12]	AT40	QPI	I
VSS	AT41	GND	
QPI0_DRX_DN[10]	AT42	QPI	I
QPI0_DRX_DP[11]	AT43	QPI	I
RSVD	AT5		
QPI1_CLKRX_DP	AT6	QPI	I
VSS	AT7	GND	
VSS	AT8	GND	
VCC	AT9	PWR	
VSS	AU1	GND	
VCC	AU10	PWR	
VSS	AU11	GND	
VCC	AU12	PWR	
VCC	AU13	PWR	
VSS	AU14	GND	
VCC	AU15	PWR	
VCC	AU16	PWR	
VSS	AU17	GND	
VCC	AU18	PWR	
VCC	AU19	PWR	
RSVD	AU2		
VSS	AU20	GND	
VCC	AU21	PWR	
VSS	AU22	GND	
VSS	AU23	GND	
VCC	AU24	PWR	
VCC	AU25	PWR	
VSS	AU26	GND	
VCC	AU27	PWR	
VCC	AU28	PWR	
VSS	AU29	GND	
QPI1_DRX_DN[8]	AU3	QPI	I
VCC	AU30	PWR	
VCC	AU31	PWR	
VSS	AU32	GND	

Table 5-2. By Land Number (Sheet 15 of

Land Name	Land No.	Buffer Type	Direction
VCC	AU33	PWR	
VCC	AU34	PWR	
VSS	AU35	GND	
VSS	AU36	GND	
QPI0_DRX_DN[0]	AU37	QPI	I
QPI0_DRX_DP[1]	AU38	QPI	I
QPI0_DRX_DP[7]	AU39	QPI	I
QPI1_DRX_DP[8]	AU4	QPI	I
QPI0_DRX_DP[9]	AU40	QPI	I
QPI0_DRX_DN[9]	AU41	QPI	I
QPI0_DRX_DP[10]	AU42	QPI	I
VSS	AU43	GND	
VSS	AU5	GND	
QPI1_DRX_DN[6]	AU6	QPI	I
QPI1_DRX_DP[6]	AU7	QPI	I
QPI1_DRX_DP[0]	AU8	QPI	I
VCC	AU9	PWR	
RSVD	AV1		
VCC	AV10	PWR	
VSS	AV11	GND	
VCC	AV12	PWR	
VCC	AV13	PWR	
VSS	AV14	GND	
VCC	AV15	PWR	
VCC	AV16	PWR	
VSS	AV17	GND	
VCC	AV18	PWR	
VCC	AV19	PWR	
RSVD	AV2		
VSS	AV20	GND	
VCC	AV21	PWR	
VSS	AV22	GND	
VSS	AV23	GND	
VCC	AV24	PWR	
VCC	AV25	PWR	
VSS	AV26	GND	
VCC	AV27	PWR	
VCC	AV28	PWR	
VSS	AV29	GND	
VTT_VID2	AV3	CMOS	O
VCC	AV30	PWR	

Table 5-2. By Land Number (Sheet 16 of

Land Name	Land No.	Buffer Type	Direction
VCC	AV31	PWR	
VSS	AV32	GND	
VCC	AV33	PWR	
VCC	AV34	PWR	
RSVD	AV35		
QPI0_DRX_DP[2]	AV36	QPI	I
QPI0_DRX_DN[2]	AV37	QPI	I
QPI0_DRX_DN[1]	AV38	QPI	I
VSS	AV39	GND	
VSS	AV4	GND	
QPI0_DRX_DN[8]	AV40	QPI	I
VSS	AV41	GND	
RSVD	AV42		
RSVD	AV43		
QPI1_DRX_DP[3]	AV5	QPI	I
VTT_VID4	AV6	CMOS	O
QPI1_DRX_DP[1]	AV7	QPI	I
QPI1_DRX_DN[0]	AV8	QPI	I
VCC	AV9	PWR	
VSS	AW1	GND	
VCC	AW10	PWR	
VSS	AW11	GND	
VCC	AW12	PWR	
VCC	AW13	PWR	
VSS	AW14	GND	
VCC	AW15	PWR	
VCC	AW16	PWR	
VSS	AW17	GND	
VCC	AW18	PWR	
VCC	AW19	PWR	
RSVD	AW2		
VSS	AW20	GND	
VCC	AW21	PWR	
VSS	AW22	GND	
VSS	AW23	GND	
VCC	AW24	PWR	
VCC	AW25	PWR	
VSS	AW26	GND	
VCC	AW27	PWR	
VCC	AW28	PWR	
VSS	AW29	GND	

Table 5-2. By Land Number (Sheet 17 of

Land Name	Land No.	Buffer Type	Direction
QPI1_DRX_DN[7]	AW3	QPI	I
VCC	AW30	PWR	
VCC	AW31	PWR	
VSS	AW32	GND	
VCC	AW33	PWR	
VCC	AW34	PWR	
VSS	AW35	GND	
QPI0_DRX_DP[3]	AW36	QPI	I
QPI0_DRX_DP[5]	AW37	QPI	I
QPI0_DRX_DN[5]	AW38	QPI	I
RSVD	AW39		
QPI1_DRX_DP[7]	AW4	QPI	I
QPI0_DRX_DP[8]	AW40	QPI	I
RSVD	AW41		
RSVD	AW42		
QPI1_DRX_DN[3]	AW5	QPI	I
VSS	AW6	GND	
QPI1_DRX_DN[1]	AW7	QPI	I
VSS	AW8	GND	
VCC	AW9	PWR	
VCC	AY10	PWR	
VSS	AY11	GND	
VCC	AY12	PWR	
VCC	AY13	PWR	
VSS	AY14	GND	
VCC	AY15	PWR	
VCC	AY16	PWR	
VSS	AY17	GND	
VCC	AY18	PWR	
VCC	AY19	PWR	
VSS	AY2	GND	
VSS	AY20	GND	
VCC	AY21	PWR	
VSS	AY22	GND	
VSS	AY23	GND	
VCC	AY24	PWR	
VCC	AY25	PWR	
VSS	AY26	GND	
VCC	AY27	PWR	
VCC	AY28	PWR	
VSS	AY29	GND	

Table 5-2. By Land Number (Sheet 18 of

Land Name	Land No.	Buffer Type	Direction
RSVD	AY3		
VCC	AY30	PWR	
VCC	AY31	PWR	
VSS	AY32	GND	
VCC	AY33	PWR	
VCC	AY34	PWR	
RSVD	AY35		
QPI0_DRX_DN[3]	AY36	QPI	I
VSS	AY37	GND	
QPI0_DRX_DN[6]	AY38	QPI	I
RSVD	AY39		
RSVD	AY4		
RSVD	AY40		
RSVD	AY41		
VSS	AY42	GND	
QPI1_DRX_DN[5]	AY5	QPI	I
QPI1_DRX_DP[5]	AY6	QPI	I
VSS	AY7	GND	
QPI1_DRX_DP[2]	AY8	QPI	I
VCC	AY9	PWR	
DDR0_CS#[1]	B10	CMOS	O
DDR0_ODT[2]	B11	CMOS	O
VDDQ	B12	PWR	
DDR0_WE#	B13	CMOS	O
DDR1_MA[13]	B14	CMOS	O
DDR0_CS#[4]	B15	CMOS	O
DDR0_BA[0]	B16	CMOS	O
VDDQ	B17	PWR	
DDR2_MA_PAR	B18	CMOS	O
DDR0_MA[10]	B19	CMOS	O
VSS	B2	GND	
DDR0_MA_PAR	B20	CMOS	O
DDR0_MA[1]	B21	CMOS	O
VDDQ	B22	PWR	
DDR0_MA[4]	B23	CMOS	O
DDR0_MA[5]	B24	CMOS	O
DDR0_MA[8]	B25	CMOS	O
DDR0_MA[12]	B26	CMOS	O
VDDQ	B27	PWR	
DDR0_PAR_ERR#[1]	B28	Asynch	I
DDR0_MA[15]	B29	CMOS	O

Table 5-2. By Land Number (Sheet 19 of

Land Name	Land No.	Buffer Type	Direction
BPM#[0]	B3	GTL	I/O
DDR0_CKE[2]	B30	CMOS	O
DDR0_CKE[3]	B31	CMOS	O
VDDQ	B32	PWR	
RSVD	B33		
DDR0_ECC[6]	B34	CMOS	I/O
DDR0_DQS_N[17]	B35	CMOS	I/O
DDR0_DQS_P[17]	B36	CMOS	I/O
VSS	B37	GND	
DDR0_DQ[31]	B38	CMOS	I/O
DDR0_DQS_P[3]	B39	CMOS	I/O
BPM#[3]	B4	GTL	I/O
DDR0_DQS_N[3]	B40	CMOS	I/O
PRDY#	B41	GTL	O
VSS	B42	GND	
DDR0_DQ[32]	B5	CMOS	I/O
DDR0_DQ[36]	B6	CMOS	I/O
VDDQ	B7	PWR	
DDR0_CS#[7]/ DDR0_ODT[5]	B8	CMOS	O
DDR0_CS#[3]	B9	CMOS	O
VCC	BA10	PWR	
VSS	BA11	GND	
VCC	BA12	PWR	
VCC	BA13	PWR	
VSS	BA14	GND	
VCC	BA15	PWR	
VCC	BA16	PWR	
VSS	BA17	GND	
VCC	BA18	PWR	
VCC	BA19	PWR	
VSS	BA20	GND	
VCC	BA24	PWR	
VCC	BA25	PWR	
VSS	BA26	GND	
VCC	BA27	PWR	
VCC	BA28	PWR	
VSS	BA29	GND	
VSS	BA3	GND	
VCC	BA30	PWR	
VSS	BA35	GND	
QPI0_DRX_DP[4]	BA36	QPI	I

Table 5-2. By Land Number (Sheet 20 of

Land Name	Land No.	Buffer Type	Direction
QPI0_DRX_DN[4]	BA37	QPI	I
QPI0_DRX_DP[6]	BA38	QPI	I
VSS	BA39	GND	
RSVD	BA4		
RSVD	BA40		
VSS	BA5	GND	
QPI1_DRX_DN[4]	BA6	QPI	I
QPI1_DRX_DP[4]	BA7	QPI	I
QPI1_DRX_DN[2]	BA8	QPI	I
VCC	BA9	PWR	
VDDQ	C10	PWR	
DDR0_CS#[6]/ DDR0_ODT[4]	C11	CMOS	O
DDR0_CAS#	C12	CMOS	O
DDR0_CS#[2]	C13	CMOS	O
DDR1_CS#[6]/ DDR1_ODT[4]	C14	CMOS	O
VDDQ	C15	PWR	
DDR2_WE#	C16	CMOS	O
DDR1_CS#[4]	C17	CMOS	O
DDR1_BA[0]	C18	CMOS	O
DDR0_CLK_N[1]	C19	CLOCK	O
BPM#[2]	C2	GTL	I/O
VDDQ	C20	PWR	
DDR1_CLK_P[0]	C21	CLOCK	O
DDR1_PAR_ERR#[0]	C22	Asynch	I
DDR0_MA[2]	C23	CMOS	O
DDR0_MA[6]	C24	CMOS	O
VDDQ	C25	PWR	
DDR0_MA[9]	C26	CMOS	O
DDR1_CKE[3]	C27	CMOS	O
DDR0_BA[2]	C28	CMOS	O
DDR0_CKE[0]	C29	CMOS	O
BPM#[5]	C3	GTL	I/O
VDDQ	C30	PWR	
RSVD	C31		
RSVD	C32		
DDR0_ECC[3]	C33	CMOS	I/O
DDR0_ECC[7]	C34	CMOS	I/O
VSS	C35	GND	
DDR0_ECC[0]	C36	CMOS	I/O
DDR0_ECC[4]	C37	CMOS	I/O

Table 5-2. By Land Number (Sheet 21 of

Land Name	Land No.	Buffer Type	Direction
DDR0_DQ[30]	C38	CMOS	I/O
DDR0_DQS_N[12]	C39	CMOS	I/O
DDR0_DQ[33]	C4	CMOS	I/O
VSS	C40	GND	
DDR0_DQ[25]	C41	CMOS	I/O
PREQ#	C42	GTL	I
VSS	C43	GND	
VSS	C5	GND	
DDR0_DQ[37]	C6	CMOS	I/O
DDR0_ODT[3]	C7	CMOS	O
DDR1_ODT[1]	C8	CMOS	O
DDR0_ODT[1]	C9	CMOS	O
BPM#[4]	D1	GTL	I/O
DDR2_ODT[3]	D10	CMOS	O
DDR1_ODT[0]	D11	CMOS	O
DDR1_CS#[0]	D12	CMOS	O
VDDQ	D13	PWR	
DDR1_ODT[2]	D14	CMOS	O
DDR2_ODT[2]	D15	CMOS	O
DDR2_CS#[2]	D16	CMOS	O
DDR2_RAS#	D17	CMOS	O
VDDQ	D18	PWR	
DDR0_CLK_P[1]	D19	CLOCK	O
BPM#[6]	D2	GTL	I/O
DDR1_MA_PAR	D20	CMOS	O
DDR1_CLK_N[0]	D21	CLOCK	O
DDR1_MA[7]	D22	CMOS	O
VDDQ	D23	PWR	
DDR0_MA[3]	D24	CMOS	O
DDR0_PAR_ERR#[0]	D25	Asynch	I
DDR2_CKE[2]	D26	CMOS	O
DDR1_CKE[2]	D27	CMOS	O
VDDQ	D28	PWR	
DDR1_RESET#	D29	CMOS	O
VSS	D3	GND	
RSVD	D30		
RSVD	D31		
DDR0_RESET#	D32	CMOS	O
VSS	D33	GND	
DDR0_DQS_P[8]	D34	CMOS	I/O
DDR0_DQS_N[8]	D35	CMOS	I/O

Table 5-2. By Land Number (Sheet 22 of

Land Name	Land No.	Buffer Type	Direction
DDR1_ECC[0]	D36	CMOS	I/O
DDR0_DQ[27]	D37	CMOS	I/O
VSS	D38	GND	
DDR0_DQS_P[12]	D39	CMOS	I/O
DDR0_DQS_N[13]	D4	CMOS	I/O
DDR0_DQ[24]	D40	CMOS	I/O
DDR0_DQ[28]	D41	CMOS	I/O
DDR0_DQ[29]	D42	CMOS	I/O
VSS	D43	GND	
DDR0_DQS_P[13]	D5	CMOS	I/O
DDR1_DQ[38]	D6	CMOS	I/O
DDR1_DQS_N[4]	D7	CMOS	I/O
VSS	D8	GND	
DDR2_CS#[5]	D9	CMOS	O
VSS	E1	GND	
DDR1_CS#[5]	E10	CMOS	O
VDDQ	E11	PWR	
DDR1_CS#[7]/ DDR1_ODT[5]	E12	CMOS	O
DDR1_CS#[3]	E13	CMOS	O
DDR1_CAS#	E14	CMOS	O
DDR1_CS#[2]	E15	CMOS	O
VDDQ	E16	PWR	
DDR2_CS#[4]	E17	CMOS	O
DDR0_CLK_N[2]	E18	CLOCK	O
DDR0_CLK_N[3]	E19	CLOCK	O
BPM#[7]	E2	GTL	I/O
DDR0_CLK_P[3]	E20	CLOCK	O
VDDQ	E21	PWR	
DDR1_MA[8]	E22	CMOS	O
DDR1_MA[11]	E23	CMOS	O
DDR1_MA[12]	E24	CMOS	O
DDR1_PAR_ERR#[1]	E25	Asynch	I
VDDQ	E26	PWR	
DDR1_CKE[1]	E27	CMOS	O
RSVD	E28		
DDR2_ECC[2]	E29	CMOS	I/O
DDR0_DQS_P[4]	E3	CMOS	I/O
DDR2_ECC[3]	E30	CMOS	I/O
VDDQ	E31	PWR	
DDR2_RESET#	E32	CMOS	O
DDR1_ECC[2]	E33	CMOS	I/O

Table 5-2. By Land Number (Sheet 23 of

Land Name	Land No.	Buffer Type	Direction
DDR1_ECC[6]	E34	CMOS	I/O
DDR1_DQS_N[17]	E35	CMOS	I/O
VSS	E36	GND	
DDR1_ECC[4]	E37	CMOS	I/O
DDR2_DQ[31]	E38	CMOS	I/O
DDR2_DQS_P[3]	E39	CMOS	I/O
DDR0_DQS_N[4]	E4	CMOS	I/O
DDR2_DQS_N[3]	E40	CMOS	I/O
VSS	E41	GND	
DDR0_DQ[18]	E42	CMOS	I/O
DDR0_DQ[19]	E43	CMOS	I/O
DDR1_DQ[34]	E5	CMOS	I/O
VSS	E6	GND	
DDR1_DQS_P[4]	E7	CMOS	I/O
DDR1_DQ[33]	E8	CMOS	I/O
DDR1_DQ[32]	E9	CMOS	I/O
DDR0_DQ[34]	F1	CMOS	I/O
DDR1_DQ[36]	F10	CMOS	I/O
DDR1_ODT[3]	F11	CMOS	O
DDR0_ODT[0]	F12	CMOS	O
DDR2_ODT[1]	F13	CMOS	O
VDDQ	F14	PWR	
DDR2_MA[13]	F15	CMOS	O
DDR2_CAS#	F16	CMOS	O
DDR2_BA[1]	F17	CMOS	O
DDR0_CLK_P[2]	F18	CLOCK	O
VDDQ	F19	PWR	
DDR0_DQ[39]	F2	CMOS	I/O
DDR2_MA[4]	F20	CMOS	O
DDR2_PAR_ERR#[0]	F21	Asynch	I
DDR1_MA[5]	F22	CMOS	O
DDR2_PAR_ERR#[2]	F23	Asynch	I
VDDQ	F24	PWR	
DDR1_PAR_ERR#[2]	F25	Asynch	I
DDR1_MA[15]	F26	CMOS	O
RSVD	F27		
RSVD	F28		
VSS	F29	GND	
DDR0_DQ[38]	F3	CMOS	I/O
DDR2_ECC[7]	F30	CMOS	I/O
DDR2_ECC[6]	F31	CMOS	I/O

Table 5-2. By Land Number (Sheet 24 of

Land Name	Land No.	Buffer Type	Direction
DDR0_ECC[2]	F32	CMOS	I/O
DDR2_ECC[1]	F33	CMOS	I/O
VSS	F34	GND	
DDR1_DQS_P[17]	F35	CMOS	I/O
DDR1_ECC[1]	F36	CMOS	I/O
DDR1_ECC[5]	F37	CMOS	I/O
DDR2_DQ[30]	F38	CMOS	I/O
VSS	F39	GND	
VSS	F4	GND	
DDR2_DQ[25]	F40	CMOS	I/O
DDR0_DQS_P[2]	F41	CMOS	I/O
DDR0_DQ[23]	F42	CMOS	I/O
DDR0_DQ[22]	F43	CMOS	I/O
DDR1_DQ[35]	F5	CMOS	I/O
DDR1_DQ[39]	F6	CMOS	I/O
DDR1_DQS_N[13]	F7	CMOS	I/O
DDR1_DQS_P[13]	F8	CMOS	I/O
VSS	F9	GND	
DDR0_DQ[44]	G1	CMOS	I/O
DDR2_DQ[37]	G10	CMOS	I/O
DDR2_DQ[36]	G11	CMOS	I/O
VSS	G12	GND	
DDR1_WE#	G13	CMOS	O
DDR1_RAS#	G14	CMOS	O
DDR0_CS#[0]	G15	CMOS	O
DDR2_CS#[0]	G16	CMOS	O
VDDQ	G17	PWR	
DDR2_MA[2]	G18	CMOS	O
DDR1_CLK_P[1]	G19	CLOCK	O
VSS	G2	GND	
DDR1_CLK_N[1]	G20	CLOCK	O
DDR2_CLK_N[2]	G21	CLOCK	O
VDDQ	G22	PWR	
DDR2_MA[12]	G23	CMOS	O
DDR1_MA[9]	G24	CMOS	O
DDR2_MA[15]	G25	CMOS	O
DDR2_CKE[1]	G26	CMOS	O
VDDQ	G27	PWR	
RSVD	G28		
DDR2_DQS_P[8]	G29	CMOS	I/O
DDR0_DQ[35]	G3	CMOS	I/O

Table 5-2. By Land Number (Sheet 25 of

Land Name	Land No.	Buffer Type	Direction
DDR2_DQS_N[8]	G30	CMOS	I/O
DDR2_DQS_N[17]	G31	CMOS	I/O
VSS	G32	GND	
DDR1_DQS_P[8]	G33	CMOS	I/O
DDR1_DQS_N[8]	G34	CMOS	I/O
DDR1_ECC[7]	G35	CMOS	I/O
DDR1_ECC[3]	G36	CMOS	I/O
VSS	G37	GND	
DDR2_DQS_N[12]	G38	CMOS	I/O
DDR2_DQ[29]	G39	CMOS	I/O
DDR1_DQ[42]	G4	CMOS	I/O
DDR2_DQ[24]	G40	CMOS	I/O
DDR0_DQS_N[2]	G41	CMOS	I/O
VSS	G42	GND	
DDR0_DQS_N[11]	G43	CMOS	I/O
DDR1_DQ[46]	G5	CMOS	I/O
DDR1_DQS_N[5]	G6	CMOS	I/O
VSS	G7	GND	
DDR1_DQ[37]	G8	CMOS	I/O
DDR1_DQ[44]	G9	CMOS	I/O
DDR0_DQ[41]	H1	CMOS	I/O
VSS	H10	GND	
DDR2_DQS_P[13]	H11	CMOS	I/O
DDR2_DQ[38]	H12	CMOS	I/O
DDR2_DQ[34]	H13	CMOS	I/O
DDR1_MA[10]	H14	CMOS	O
VDDQ	H15	PWR	
DDR2_CS#[3]	H16	CMOS	O
DDR2_MA[10]	H17	CMOS	O
DDR1_CLK_P[3]	H18	CLOCK	O
DDR1_CLK_N[3]	H19	CLOCK	O
DDR0_DQ[40]	H2	CMOS	I/O
VDDQ	H20	PWR	
DDR2_CLK_P[2]	H21	CLOCK	O
DDR2_MA[9]	H22	CMOS	O
DDR2_MA[11]	H23	CMOS	O
DDR2_MA[14]	H24	CMOS	O
VDDQ	H25	PWR	
DDR1_MA[14]	H26	CMOS	O
DDR1_BA[2]	H27	CMOS	O
DDR1_CKE[0]	H28	CMOS	O

Table 5-2. By Land Number (Sheet 26 of

Land Name	Land No.	Buffer Type	Direction
RSVD	H29		
DDR0_DQ[45]	H3	CMOS	I/O
VSS	H30	GND	
DDR2_DQS_P[17]	H31	CMOS	I/O
DDR2_ECC[0]	H32	CMOS	I/O
DDR1_DQ[24]	H33	CMOS	I/O
DDR1_DQ[29]	H34	CMOS	I/O
VSS	H35	GND	
DDR1_DQ[23]	H36	CMOS	I/O
DDR2_DQ[27]	H37	CMOS	I/O
DDR2_DQS_P[12]	H38	CMOS	I/O
DDR2_DQ[28]	H39	CMOS	I/O
DDR1_DQ[43]	H4	CMOS	I/O
VSS	H40	GND	
DDR0_DQ[16]	H41	CMOS	I/O
DDR0_DQS_P[11]	H42	CMOS	I/O
DDR0_DQ[17]	H43	CMOS	I/O
VSS	H5	GND	
DDR1_DQS_P[5]	H6	CMOS	I/O
DDR1_DQS_P[14]	H7	CMOS	I/O
DDR1_DQ[40]	H8	CMOS	I/O
DDR1_DQ[45]	H9	CMOS	I/O
DDR0_DQS_N[14]	J1	CMOS	I/O
DDR2_DQS_P[4]	J10	CMOS	I/O
DDR2_DQS_N[13]	J11	CMOS	I/O
DDR2_DQ[33]	J12	CMOS	I/O
VSS	J13	GND	
DDR1_MA[0]	J14	CMOS	O
DDR2_CS#[7]/ DDR2_ODT[5]	J15	CMOS	O
DDR1_MA[1]	J16	CMOS	O
DDR1_MA[2]	J17	CMOS	O
VDDQ	J18	PWR	
DDR0_CLK_P[0]	J19	CLOCK	O
DDR0_DQS_P[14]	J2	CMOS	I/O
DDR2_MA[3]	J20	CMOS	O
DDR2_CLK_N[0]	J21	CLOCK	O
DDR2_CLK_P[0]	J22	CLOCK	O
VDDQ	J23	PWR	
DDR2_MA[7]	J24	CMOS	O
DDR2_PAR_ERR#[1]	J25	Asynch	I
DDR2_CKE[0]	J26	CMOS	O

Table 5-2. By Land Number (Sheet 27 of

Land Name	Land No.	Buffer Type	Direction
DDR1_MA[6]	J27	CMOS	O
VDDQ	J28	PWR	
RSVD	J29		
VSS	J3	GND	
DDR2_ECC[5]	J30	CMOS	I/O
DDR2_ECC[4]	J31	CMOS	I/O
DDR1_DQ[27]	J32	CMOS	I/O
VSS	J33	GND	
DDR1_DQ[28]	J34	CMOS	I/O
DDR1_DQ[19]	J35	CMOS	I/O
DDR1_DQ[22]	J36	CMOS	I/O
DDR2_DQ[26]	J37	CMOS	I/O
VSS	J38	GND	
DDR2_DQ[19]	J39	CMOS	I/O
DDR1_DQ[52]	J4	CMOS	I/O
DDR2_DQ[18]	J40	CMOS	I/O
DDR0_DQ[21]	J41	CMOS	I/O
DDR0_DQ[20]	J42	CMOS	I/O
VSS	J43	GND	
DDR1_DQ[47]	J5	CMOS	I/O
DDR1_DQ[41]	J6	CMOS	I/O
DDR1_DQS_N[14]	J7	CMOS	I/O
VSS	J8	GND	
DDR2_DQS_N[4]	J9	CMOS	I/O
VSS	K1	GND	
DDR2_DQ[41]	K10	CMOS	I/O
VSS	K11	GND	
DDR2_DQ[32]	K12	CMOS	I/O
DDR1_BA[1]	K13	CMOS	O
DDR2_CS#[1]	K14	CMOS	O
RSVD	K15		
VDDQ	K16	PWR	
DDR2_MA[1]	K17	CMOS	O
DDR1_CLK_P[2]	K18	CLOCK	O
DDR0_CLK_N[0]	K19	CLOCK	O
DDR0_DQS_P[5]	K2	CMOS	I/O
DDR2_CLK_N[1]	K20	CLOCK	O
VDDQ	K21	PWR	
DDR2_MA[6]	K22	CMOS	O
DDR2_MA[5]	K23	CMOS	O
RSVD	K24		

Table 5-2. By Land Number (Sheet 28 of

Land Name	Land No.	Buffer Type	Direction
RSVD	K25		
VDDQ	K26	PWR	
RSVD	K27		
DDR1_MA[4]	K28	CMOS	O
RSVD	K29		
DDR0_DQS_N[5]	K3	CMOS	I/O
DDR1_DQ[31]	K30	CMOS	I/O
VSS	K31	GND	
DDR1_DQ[26]	K32	CMOS	I/O
DDR1_DQS_N[12]	K33	CMOS	I/O
DDR1_DQS_P[12]	K34	CMOS	I/O
DDR1_DQ[18]	K35	CMOS	I/O
VSS	K36	GND	
DDR1_DQS_N[11]	K37	CMOS	I/O
DDR2_DQ[23]	K38	CMOS	I/O
DDR2_DQS_N[2]	K39	CMOS	I/O
DDR1_DQ[48]	K4	CMOS	I/O
DDR2_DQS_P[2]	K40	CMOS	I/O
VSS	K41	GND	
DDR0_DQ[10]	K42	CMOS	I/O
DDR0_DQ[11]	K43	CMOS	I/O
DDR1_DQ[49]	K5	CMOS	I/O
VSS	K6	GND	
DDR2_DQS_N[5]	K7	CMOS	I/O
DDR2_DQS_N[14]	K8	CMOS	I/O
DDR2_DQS_P[14]	K9	CMOS	I/O
DDR0_DQ[42]	L1	CMOS	I/O
DDR2_DQ[40]	L10	CMOS	I/O
DDR2_DQ[44]	L11	CMOS	I/O
DDR2_DQ[39]	L12	CMOS	I/O
DDR2_DQ[35]	L13	CMOS	I/O
VDDQ	L14	PWR	
RSVD	L15		
DDR2_ODT[0]	L16	CMOS	O
DDR2_CS#[6]/ DDR2_ODT[4]	L17	CMOS	O
DDR1_CLK_N[2]	L18	CLOCK	O
VDDQ	L19	PWR	
DDR0_DQ[47]	L2	CMOS	I/O
DDR2_CLK_P[1]	L20	CLOCK	O
DDR2_CLK_N[3]	L21	CLOCK	O
DDR2_CLK_P[3]	L22	CLOCK	O

Table 5-2. By Land Number (Sheet 29 of

Land Name	Land No.	Buffer Type	Direction
DDR_VREF	L23	Analog	I
VDDQ	L24	PWR	
DDR2_MA[8]	L25	CMOS	O
DDR2_BA[2]	L26	CMOS	O
DDR2_CKE[3]	L27	CMOS	O
DDR1_MA[3]	L28	CMOS	O
VSS	L29	GND	
DDR0_DQ[46]	L3	CMOS	I/O
DDR1_DQS_P[3]	L30	CMOS	I/O
DDR1_DQS_N[3]	L31	CMOS	I/O
DDR1_DQ[30]	L32	CMOS	I/O
DDR1_DQ[25]	L33	CMOS	I/O
VSS	L34	GND	
DDR1_DQS_P[2]	L35	CMOS	I/O
DDR1_DQS_N[2]	L36	CMOS	I/O
DDR1_DQS_P[11]	L37	CMOS	I/O
DDR2_DQS_N[11]	L38	CMOS	I/O
VSS	L39	GND	
VSS	L4	GND	
DDR2_DQ[22]	L40	CMOS	I/O
DDR0_DQS_P[1]	L41	CMOS	I/O
DDR0_DQ[15]	L42	CMOS	I/O
DDR0_DQ[14]	L43	CMOS	I/O
DDR1_DQS_N[6]	L5	CMOS	I/O
DDR1_DQS_P[6]	L6	CMOS	I/O
DDR2_DQS_P[5]	L7	CMOS	I/O
DDR2_DQ[46]	L8	CMOS	I/O
VSS	L9	GND	
DDR0_DQ[43]	M1	CMOS	I/O
DDR2_DQ[45]	M10	CMOS	I/O
VCC	M11	PWR	
VSS	M12	GND	
VCC	M13	PWR	
VSS	M14	GND	
VCC	M15	PWR	
VSS	M16	GND	
VDDQ	M17	PWR	
VSS	M18	GND	
VCC	M19	PWR	
VSS	M2	GND	
VSS	M20	GND	

Table 5-2. By Land Number (Sheet 30 of

Land Name	Land No.	Buffer Type	Direction
VCC	M21	PWR	
VSS	M22	GND	
VCC	M23	PWR	
VSS	M24	GND	
VCC	M25	PWR	
VSS	M26	GND	
VDDQ	M27	PWR	
VSS	M28	GND	
VCC	M29	PWR	
DDR0_DQ[52]	M3	CMOS	I/O
VSS	M30	GND	
VCC	M31	PWR	
VSS	M32	GND	
VCC	M33	PWR	
DDR1_DQ[17]	M34	CMOS	I/O
DDR1_DQ[16]	M35	CMOS	I/O
DDR1_DQ[21]	M36	CMOS	I/O
VSS	M37	GND	
DDR2_DQS_P[11]	M38	CMOS	I/O
DDR2_DQ[16]	M39	CMOS	I/O
DDR1_DQS_N[15]	M4	CMOS	I/O
DDR2_DQ[17]	M40	CMOS	I/O
DDR0_DQS_N[1]	M41	CMOS	I/O
VSS	M42	GND	
DDR0_DQS_N[10]	M43	CMOS	I/O
DDR1_DQS_P[15]	M5	CMOS	I/O
DDR1_DQ[53]	M6	CMOS	I/O
VSS	M7	GND	
DDR2_DQ[47]	M8	CMOS	I/O
DDR2_DQ[42]	M9	CMOS	I/O
DDR0_DQ[48]	N1	CMOS	I/O
VSS	N10	GND	
VCC	N11	PWR	
DDR0_DQ[49]	N2	CMOS	I/O
DDR0_DQ[53]	N3	CMOS	I/O
VCC	N33	PWR	
DDR1_DQ[20]	N34	CMOS	I/O
VSS	N35	GND	
DDR2_DQ[21]	N36	CMOS	I/O
DDR1_DQ[14]	N37	CMOS	I/O
DDR1_DQ[15]	N38	CMOS	I/O

Table 5-2. By Land Number (Sheet 31 of

Land Name	Land No.	Buffer Type	Direction
DDR1_DQ[11]	N39	CMOS	I/O
DDR2_DQS_P[15]	N4	CMOS	I/O
VSS	N40	GND	
DDR0_DQ[8]	N41	CMOS	I/O
DDR0_DQS_P[10]	N42	CMOS	I/O
DDR0_DQ[9]	N43	CMOS	I/O
VSS	N5	GND	
DDR2_DQ[49]	N6	CMOS	I/O
DDR2_DQ[53]	N7	CMOS	I/O
DDR2_DQ[52]	N8	CMOS	I/O
DDR2_DQ[43]	N9	CMOS	I/O
DDR0_DQS_N[15]	P1	CMOS	I/O
DDR2_DQ[51]	P10	CMOS	I/O
VSS	P11	GND	
DDR0_DQS_P[15]	P2	CMOS	I/O
VSS	P3	GND	
VSS	P33	GND	
DDR1_DQ[8]	P34	CMOS	I/O
DDR1_DQ[9]	P35	CMOS	I/O
DDR1_DQS_P[10]	P36	CMOS	I/O
DDR1_DQS_N[10]	P37	CMOS	I/O
VSS	P38	GND	
DDR1_DQ[10]	P39	CMOS	I/O
DDR2_DQS_N[15]	P4	CMOS	I/O
DDR2_DQ[20]	P40	CMOS	I/O
DDR0_DQ[13]	P41	CMOS	I/O
DDR0_DQ[12]	P42	CMOS	I/O
VSS	P43	GND	
DDR2_DQS_N[6]	P5	CMOS	I/O
DDR2_DQS_P[6]	P6	CMOS	I/O
DDR2_DQ[48]	P7	CMOS	I/O
VSS	P8	GND	
DDR2_DQ[50]	P9	CMOS	I/O
VSS	R1	GND	
DDR2_DQ[54]	R10	CMOS	I/O
VCC	R11	PWR	
DDR0_DQS_P[6]	R2	CMOS	I/O
DDR0_DQS_N[6]	R3	CMOS	I/O
VCC	R33	PWR	
DDR1_DQ[12]	R34	CMOS	I/O
DDR1_DQ[13]	R35	CMOS	I/O

Table 5-2. By Land Number (Sheet 32 of

Land Name	Land No.	Buffer Type	Direction
VSS	R36	GND	
DDR1_DQS_N[1]	R37	CMOS	I/O
DDR1_DQS_P[1]	R38	CMOS	I/O
DDR2_DQ[10]	R39	CMOS	I/O
DDR0_DQ[54]	R4	CMOS	I/O
DDR2_DQ[15]	R40	CMOS	I/O
VSS	R41	GND	
DDR0_DQ[3]	R42	CMOS	I/O
DDR0_DQ[2]	R43	CMOS	I/O
DDR1_DQ[50]	R5	CMOS	I/O
VSS	R6	GND	
DDR1_DQ[55]	R7	CMOS	I/O
DDR1_DQ[54]	R8	CMOS	I/O
DDR2_DQ[55]	R9	CMOS	I/O
DDR0_DQ[50]	T1	CMOS	I/O
DDR2_DQ[58]	T10	CMOS	I/O
VCC	T11	PWR	
DDR0_DQ[51]	T2	CMOS	I/O
DDR0_DQ[55]	T3	CMOS	I/O
VCC	T33	PWR	
VSS	T34	GND	
DDR2_DQS_N[9]	T35	CMOS	I/O
DDR2_DQ[11]	T36	CMOS	I/O
DDR2_DQS_P[1]	T37	CMOS	I/O
DDR2_DQS_N[1]	T38	CMOS	I/O
VSS	T39	GND	
VSS	T4	GND	
DDR2_DQS_N[10]	T40	CMOS	I/O
DDR2_DQ[14]	T41	CMOS	I/O
DDR0_DQ[7]	T42	CMOS	I/O
DDR0_DQS_P[0]	T43	CMOS	I/O
DDR1_DQ[51]	T5	CMOS	I/O
DDR2_DQ[60]	T6	CMOS	I/O
DDR2_DQ[61]	T7	CMOS	I/O
DDR2_DQS_N[7]	T8	CMOS	I/O
VSS	T9	GND	
DDR0_DQ[60]	U1	CMOS	I/O
DDR2_DQ[59]	U10	CMOS	I/O
RSVD	U11		
VSS	U2	GND	
DDR0_DQ[61]	U3	CMOS	I/O

Table 5-2. By Land Number (Sheet 33 of

Land Name	Land No.	Buffer Type	Direction
VCCPLL	U33	PWR	
DDR2_DQ[4]	U34	CMOS	I/O
DDR2_DQS_P[9]	U35	CMOS	I/O
DDR2_DQ[3]	U36	CMOS	I/O
VSS	U37	GND	
DDR2_DQ[8]	U38	CMOS	I/O
DDR2_DQ[9]	U39	CMOS	I/O
DDR0_DQ[56]	U4	CMOS	I/O
DDR2_DQS_P[10]	U40	CMOS	I/O
DDR0_DQ[6]	U41	CMOS	I/O
VSS	U42	GND	
DDR0_DQS_N[0]	U43	CMOS	I/O
DDR2_DQ[56]	U5	CMOS	I/O
DDR2_DQ[57]	U6	CMOS	I/O
VSS	U7	GND	
DDR2_DQS_P[7]	U8	CMOS	I/O
DDR2_DQ[63]	U9	CMOS	I/O
DDR0_DQ[57]	V1	CMOS	I/O
VSS	V10	GND	
RSVD	V11		
DDR0_DQS_P[16]	V2	CMOS	I/O
DDR0_DQS_N[16]	V3	CMOS	I/O
VCCPLL	V33	PWR	
DDR2_DQ[5]	V34	CMOS	I/O
VSS	V35	GND	
DDR2_DQ[2]	V36	CMOS	I/O
DDR2_DQ[6]	V37	CMOS	I/O
DDR2_DQ[7]	V38	CMOS	I/O
DDR2_DQ[13]	V39	CMOS	I/O
DDR0_DQ[62]	V4	CMOS	I/O
VSS	V40	GND	
DDR0_DQ[1]	V41	CMOS	I/O
DDR0_DQS_N[9]	V42	CMOS	I/O
DDR0_DQS_P[9]	V43	CMOS	I/O
VSS	V5	GND	
DDR2_DQS_P[16]	V6	CMOS	I/O
DDR2_DQS_N[16]	V7	CMOS	I/O
DDR2_DQ[62]	V8	CMOS	I/O
DDR1_DQ[60]	V9	CMOS	I/O
DDR0_DQS_N[7]	W1	CMOS	I/O
DDR1_DQ[59]	W10	CMOS	I/O

Table 5-2. By Land Number (Sheet 34 of

Land Name	Land No.	Buffer Type	Direction
VCC	W11	PWR	
DDR0_DQS_P[7]	W2	CMOS	I/O
VSS	W3	GND	
VCCPLL	W33	PWR	
DDR2_DQ[0]	W34	CMOS	I/O
DDR2_DQ[1]	W35	CMOS	I/O
DDR2_DQS_N[0]	W36	CMOS	I/O
DDR2_DQS_P[0]	W37	CMOS	I/O
VSS	W38	GND	
DDR2_DQ[12]	W39	CMOS	I/O
DDR0_DQ[63]	W4	CMOS	I/O
DDR0_DQ[4]	W40	CMOS	I/O
DDR0_DQ[0]	W41	CMOS	I/O
DDR0_DQ[5]	W42	CMOS	I/O
VSS	W43	GND	
DDR1_DQ[61]	W5	CMOS	I/O
DDR1_DQ[56]	W6	CMOS	I/O
DDR1_DQ[57]	W7	CMOS	I/O
VSS	W8	GND	
DDR1_DQ[63]	W9	CMOS	I/O
VSS	Y1	GND	
DDR1_DQ[58]	Y10	CMOS	I/O
VSS	Y11	GND	
DDR0_DQ[58]	Y2	CMOS	I/O
DDR0_DQ[59]	Y3	CMOS	I/O
VSS	Y33	GND	
DDR1_DQ[3]	Y34	CMOS	I/O
DDR1_DQ[2]	Y35	CMOS	I/O
VSS	Y36	GND	
DDR1_DQS_N[0]	Y37	CMOS	I/O
DDR1_DQS_P[0]	Y38	CMOS	I/O
DDR1_DQ[7]	Y39	CMOS	I/O
DDR1_DQS_P[16]	Y4	CMOS	I/O
DDR1_DQ[6]	Y40	CMOS	I/O
VSS	Y41	GND	
DDR1_DQS_N[16]	Y5	CMOS	I/O

Table 5-2. By Land Number (Sheet 35 of

Land Name	Land No.	Buffer Type	Direction
VSS	Y6	GND	
DDR_COMP[1]	Y7	Analog	
DDR1_DQS_P[7]	Y8	CMOS	I/O
DDR1_DQS_N[7]	Y9	CMOS	I/O

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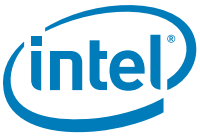

6 Signal Definitions

6.1 Signal Definitions

Table 6-1. Signal Definitions (Sheet 1 of 4)

Name	Type	Description	Notes
BCLK_DN BCLK_DP	I	Differential bus clock input to the processor.	
BCLK_ITP_DN BCLK_ITP_DP	O	Buffered differential bus clock pair to ITP.	
BPM#[7:0]	I/O	BPM#[7:0] are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM#[7:0] should be connected in a wired OR topology between all packages on a platform. BPM#[5] and BPM#[7] signals between the two processors must remain connected on production units.	
CAT_ERR#	I/O	Indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this for non-recoverable machine check errors and other internal unrecoverable error. It is expected that every processor in the system will have this hooked up in a wired-OR configuration. Since this is an I/O pin, external agents are allowed to assert this pin which will cause the processor to take a machine check exception. On Intel Xeon processor 5600 series, CAT_ERR# is used for signalling the following types of errors: • Legacy MCERR's, CAT_ERR# is pulsed for 16 BCLKs. • Legacy IERR's, CAT_ERR remains asserted until warm or cold reset.	
COMP0	I	Impedance Compensation must be terminated on the system board using precision resistor.	
QPI0_CLKRX_DN QPI0_CLKRX_DP	I I	Intel QuickPath Interconnect received clock is the input clock that corresponds to Intel QuickPath Interconnect port0 received data.	
QPI0_CLKTX_DN QPI0_CLKTX_DP	O O	Intel QuickPath Interconnect forwarded clock sent with Intel QuickPath Interconnect 0 port outbound data.	
QPI0_COMP	I	Must be terminated on the system board using precision resistor.	
QPI0_DRX_DN[19:0] QPI0_DRX_DP[19:0]	I I	QPI0_DRX_DN[19:0] and QPI0_DRX_DP[19:0] comprise the differential receive data for Intel QuickPath Interconnect port0. The inbound 20 lanes are connected to another component's outbound lanes.	
QPI0_DTX_DN[19:0] QPI0_DTX_DP[19:0]	O O	QPI0_DTX_DN[19:0] and QPI0_DTX_DP[19:0] comprise the differential transmit data for Intel QuickPath Interconnect port0. The outbound 20 lanes are connected to another component's inbound lanes.	
QPI1_CLKRX_DN QPI1_CLKRX_DP	I I	Intel QuickPath Interconnect received clock is the input clock that corresponds to Intel QuickPath Interconnect 1 port received data.	
QPI1_CLKTX_DN QPI1_CLKTX_DP	O O	Intel QuickPath Interconnect forwarded clock sent with Intel QuickPath Interconnect port1 outbound data.	
QPI1_COMP	I	Must be terminated on the system board using precision resistor.	
QPI1_DRX_DN[19:0] QPI1_DRX_DP[19:0]	I I	QPI1_DRX_DN[19:0] and QPI1_DRX_DP[19:0] comprise the differential receive data for Intel QuickPath Interconnect port1. The inbound 20 lanes are connected to another component's outbound lanes.	
QPI1_DTX_DN[19:0] QPI1_DTX_DP[19:0]	O O	QPI1_DTX_DN[19:0] and QPI1_DTX_DP[19:0] comprise the differential transmit data for Intel QuickPath Interconnect port1. The outbound 20 lanes are connected to another component's inbound lanes.	

Table 6-1. Signal Definitions (Sheet 2 of 4)

Name	Type	Description	Notes
DBR#	I	DBR# is used only in systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset.	
DDR_COMP[2:0]	I	Must be terminated on the system board using precision resistors.	
DDR_THERM#	I	DDR_THERM# is used for imposing duty cycle throttling on all memory channels. The platform should ensure that DDR_THERM# is asserted when any DIMM is over T64.	
DDR_THERM2#	I	DDR_THERM2# is used for imposing duty cycle throttling on all memory channels or implementing 2X Refresh.	
DDR{0/1/2}_BA[2:0]	O	Defines the bank which is the destination for the current Activate, Read, Write, or Precharge command.	1
DDR{0/1/2}_CAS#	O	Column Address Strobe.	
DDR{0/1/2}_CKE[3:0]	O	Clock Enable.	
DDR{0/1/2}_CLK_N[3:0] DDR{0/1/2}_CLK_P[3:0]	O	Differential clocks to the DIMM. All command and control signals are valid on the rising edge of clock.	
DDR{0/1/2}_CS[7:0]#	O	Each signal selects one rank as the target of the command and address.	
DDR{0/1/2}_DQ[63:0]	I/O	DDR3 Data bits.	
DDR{0/1/2}_DQS_N[17:0] DDR{0/1/2}_DQS_P[17:0]	I/O	Differential pair, Data/ECC Strobe. Differential strobes latch data/ECC for each DRAM. Different numbers of strobes are used depending on whether the connected DRAMs are x4,x8. Driven with edges in center of data, receive edges are aligned with data edges.	
DDR{0/1/2}_ECC[7:0]	I/O	Check Bits - An Error Correction Code is driven along with data on these lines for DIMMs that support that capability.	
DDR{0/1/2}_MA[15:0]	O	Selects the Row address for Reads and writes, and the column address for activates. Also used to set values for DRAM configuration registers.	
DDR{0/1/2}_MA_PAR	O	Odd parity across Address and Command.	
DDR{0/1/2}_ODT[3:0]	O	Enables various combinations of termination resistance in the target and non-target DIMMs when data is read or written	
DDR{0/1/2}_PAR_ERR#[2:0]	I	Parity Error detected by Registered DIMM (one for each DIMM).	
DDR{0/1/2}_RAS#	O	Row Address Strobe.	
DDR{0/1/2}_RESET#	O	Resets DRAMs. Held low on power up, held high during self refresh, otherwise controlled by configuration register.	
DDR_VREF	I	Voltage reference for DDR3.	
DDR{0/1/2}_WE#	O	Write Enable.	
GTLREF	I	Voltage reference for GTL signals.	
ISENSE	I	Analog input voltage with respect to VSS for sensing core current consumption, comes from VR11.1.	
PECI	I/O	PECI (Platform Environment Control Interface) is the serial sideband interface to the processor and is used primarily for thermal, power and error management.	
PECI_ID#	I	PECI_ID# is the PECI client address identifier. This pin is active low and asserted when tied to VSS. Assertion of this pin results in a PECI client address of 0x31 (versus the default 0x30 client address). This pin is primarily useful for PECI client address differentiation in DP platforms and must be pulled up to VTT on one socket and down to VSS on the other.	
PRDY#	O	PRDY# is a processor output used by debug tools to determine processor debug readiness.	
PREQ#	I/O	PREQ# is used by debug tools to request debug operation of the processor.	

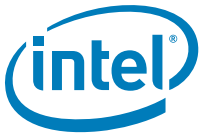

Table 6-1. Signal Definitions (Sheet 3 of 4)

Name	Type	Description	Notes
PROCHOT#	I/O	PROCHOT# will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal can also be driven to the processor to activate the Thermal Control Circuit. If PROCHOT# is asserted at the deassertion of RESET# on DP enabled products, the processor will tri-state its outputs. This signal does not have on-die termination and must be terminated on the system board.	
PSI#	O	Processor Power Status Indicator signal. This signal is asserted when maximum possible processor core current consumption is less than 20A, Assertion of this signal is an indication that the VR controller does not currently need to be able to provide ICC above 20A, and the VR controller can use this information to move to more efficient operation point.	
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. Note some PLL, Intel QuickPath Interconnect and error states are not affected by reset and only VCCPWRGOOD forces them to a known state. For a power-on Reset, RESET# must stay active for at least one millisecond after VCC and BCLK have reached their proper specifications. RESET# must not be kept asserted for more than 10 ms while VCCPWRGOOD is asserted. RESET# must be held deasserted for at least one millisecond before it is asserted again. RESET# must be held asserted before VCCPWRGOOD is asserted. This signal does not have on-die termination and must be terminated on the system board. RESET# is a common clock signal.	
SKTOCC#	O	Socket occupied. The platform designer can use this signal to enable power supplies when there is a CPU occupying the socket. Requires external pull-up.	
TAPPWRGOOD	O	Processor output signal, which when deasserted indicates the processor is in a low power state and TAP functionality is unavailable.	
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).	
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.	
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.	
THERMTRIP#	O	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor. Once activated, the processor will stop all execution and shut down all PLLs. To further protect the processor, its core voltage (V_{CC}), V_{TTA} V_{TTD} and V_{DDQ} must be removed following the assertion of THERMTRIP#. See Figure 2-27 and Figure 2-27 for the appropriate power down sequence and timing requirements. Once activated, THERMTRIP# remains latched until RESET# is asserted. While the assertion of the RESET# signal may de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted after RESET# is de-asserted.	
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.	
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.	
VCC_SENSE VSS_SENSE	O O	VCC_SENSE and VSS_SENSE provide an isolated, low impedance connection to the processor core voltage and ground. They can used to sense or measure power near the silicon with little noise.	
V_{CC}	I	Power for processor core.	

Table 6-1. Signal Definitions (Sheet 4 of 4)

Name	Type	Description	Notes
VCCPWRGOOD	I	VCCPWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that BCLK, V_{CC}, V_{CCPLL}, V_{TTA} and V_{TTD} supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. VCCPWRGOOD can be driven inactive at any time, but BCLK and power must again be stable before a subsequent rising edge of VCCPWRGOOD. In addition at the time VCCPWRGOOD is asserted RESET# must be active. The VCCPWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.	
V_{CCPLL}	I	Analog Power for Clocks.	
V_{DDQ}	I	Power supply for the DDR3 interface.	
VTT_VID[4:2]	O	VTT_VID[4:2] is used to support automatic selection of power supply voltages (V_{TT}). The voltage supply for this signal must be valid before the VR can supply V_{TT} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID signal become valid. The VID signal is needed to support the processor voltage specification variations. The VR must supply the voltage that is requested by the signal.	
V_{TTA}	I	Power for the analog portion of the Intel QuickPath and Shared Cache.	
V_{TTD}	I	Power for the digital portion of the Intel QuickPath and Shared Cache.	
VDDPWRGOOD	I	VDDPWRGOOD is an input that indicates the VDDQ power supply is good. The processor requires this signal to be a clean indication that the Vddq power supply is stable and within their specifications. "Clean" implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the VDDQ supply is turned on until it comes within specification. The signals must then transition monotonically to a high state. The VDDPWRGOOD signal must be supplied to the processor. This signal is used to protect internal circuits against voltage sequencing issues.	
VID[7:0]	I/O	VID[7:0] (Voltage ID) are output signals that are used to support automatic selection of power supply voltages (V_{CC}). The voltage supply for these signals must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID signals become valid. The VID signals are needed to support the processor voltage specification variations. The VR must supply the voltage that is requested by the signals, or disable itself. MSID[2:0] - Market Segment ID, or MSID are provided to indicate the Market Segment for the processor and may be used for future processor compatibility or for keying. In addition, MSID protects the platform by preventing a higher power processor from booting in a platform designed for lower power processors. This value is latched from the platform in to the CPU, on the rising edge of VTTPWRGOOD, during the cold boot power up sequence. CSC[2:0] - Current Sense Configuration bits are output signals for ISENSE gain setting.This value is latched on the rising edge of VTTPWRGOOD.	2
V_{TTD_SENSE} $V_{SS\_SENSE\_VTT}$	O O	V_{TTD_SENSE} and $V_{SS\_SENSE\_VTT}$ provide an isolated, low impedance connection to the processor core power and ground. They can used to sense or measure power near the silicon.	
VTTPWRGOOD	I	The processor requires this input signal to be a clean indication that the VTT power supply is stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. to determine that the VTT voltage is stable and within specification. Note it is not valid for VTTPWRGOOD to be deasserted while VCCPWRGOOD is asserted.	

Notes:

1. DDR{0/1/2} refers to DDR3 Channel 0, DDR3 Channel 1, and DDR3 Channel 2.
2. VID[7:0] is an Input only during Power On Configuration. It is an Output signal during normal operation.

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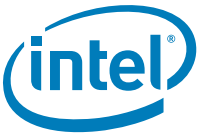


7 Thermal Specifications

7.1 Package Thermal Specifications

The processor requires a thermal solution to maintain temperatures within operating limits. Any attempt to operate the processor outside these limits may result in permanent damage to the processor and potentially other components within the system. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor integrated heat spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

This section provides data necessary for developing a complete thermal solution. For more information on designing a component level thermal solution, refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines*.

Note: The boxed processor will ship with a component thermal solution. Refer to Section 9 for details on the boxed processor.

7.1.1 Thermal Specifications

To allow optimal operation and long-term reliability of Intel processor-based systems, the processor must remain within the minimum and maximum case temperature (T_{CASE}) specifications as defined by the applicable thermal profile. Thermal solutions not designed to provide sufficient thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, please refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines*.

The processors implement a methodology for managing processor temperatures which is intended to support acoustic noise reduction through fan speed control and to assure processor reliability. Selection of the appropriate fan speed is based on the relative temperature data reported by the processor's Platform Environment Control Interface (PECI) as described in Section 7.3. If PECI is less than TCONTROL, then the case temperature is permitted to exceed the Thermal Profile, but PECI must remain at or below TCONTROL. If PECI >= TCONTROL, then the case temperature must meet the Thermal Profile. The temperature reported over PECI is always a negative value and represents a delta below the onset of thermal control circuit (TCC) activation, as indicated by PROCHOT# (see Section 7.2, Processor Thermal Features). Systems that implement fan speed control must be designed to use this data. Systems that do not alter the fan speed only need to guarantee the case temperature meets the thermal profile specifications.

Thermal Profiles are broken out separately for the Intel® Xeon® processor 5600 series 6-core and 4-core SKUs. This reflects different Thermal Test Vehicle (TTV) Correction Factors (CFs), resulting from different power density characteristics associated with the different number of cores. There is no difference in platform thermal solution assumptions or boundary conditions between the 6-core and 4-core SKUs for a given FMB (e.g., 130W). For the latest TTV CFs, please refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines*.

The processor Advanced Server/Workstation Platform supports dual thermal profiles, either of which can be implemented. Both ensure adherence to Intel reliability requirements. Thermal Profile A is representative of a volumetrically unconstrained thermal solution (that is, industry enabled 2U heatsink). In this scenario, it is expected that the Thermal Control Circuit (TCC) would only be activated for very brief periods of time when running the most power intensive applications. Thermal Profile B is indicative of a constrained thermal environment (that is, 1U form factor). Because of the reduced cooling capability represented by this thermal solution, the probability of TCC activation and performance loss is increased. Additionally, utilization of a thermal solution that does not meet Thermal Profile B will violate the thermal specifications and may result in permanent damage to the processor. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for details on system thermal solution design, thermal profiles and environmental considerations.

The upper point of the thermal profile consists of the Thermal Design Power (TDP) and the associated T_{CASE} value. It should be noted that the upper point associated with Thermal Profile B (x = TDP and y = $T_{CASE\_MAX\_B}$ @ TDP) represents a thermal solution design point. In actuality the processor case temperature will not reach this value due to TCC activation.

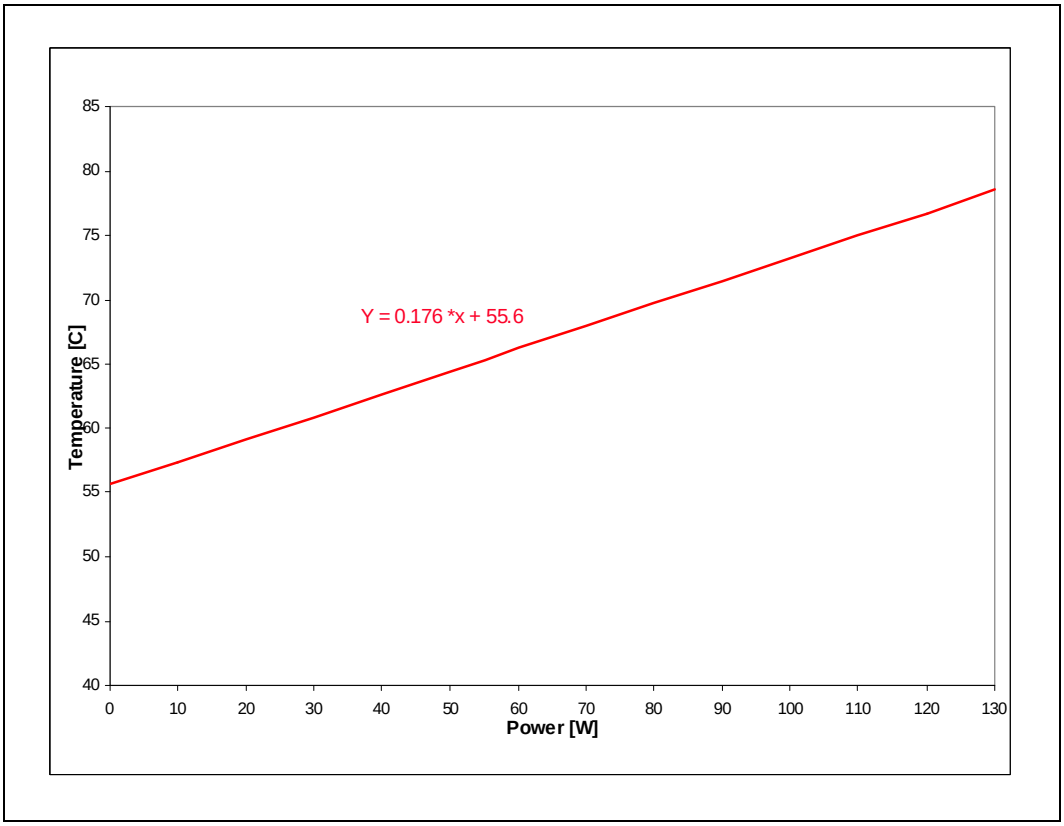
Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP). The Adaptive Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. To ensure maximum flexibility for future requirements, systems should be designed to the Flexible Motherboard (FMB) guidelines, even if a processor with lower power dissipation is currently planned. **The Adaptive Thermal Monitor feature must be enabled for the processor to remain within its specifications.**

Table 7-1. Frequency Optimized Server/Workstation Platform Thermal Specifications

Core Frequency	Thermal Design Power (W)	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)	Notes
Launch to FMB	130	5	See Figure 7-1; Table 7-2; Figure 7-2; Table 7-3	1, 2, 3, 4

Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified ICC. Please refer to the electrical loadline specifications in Section 2.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. Power specifications are defined at all VIDs found in Table 2-2. The processor may be delivered under multiple VIDs for each frequency.
4. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 7-1. Frequency Optimized Server / Workstation Platform Thermal Profile (6 Core)



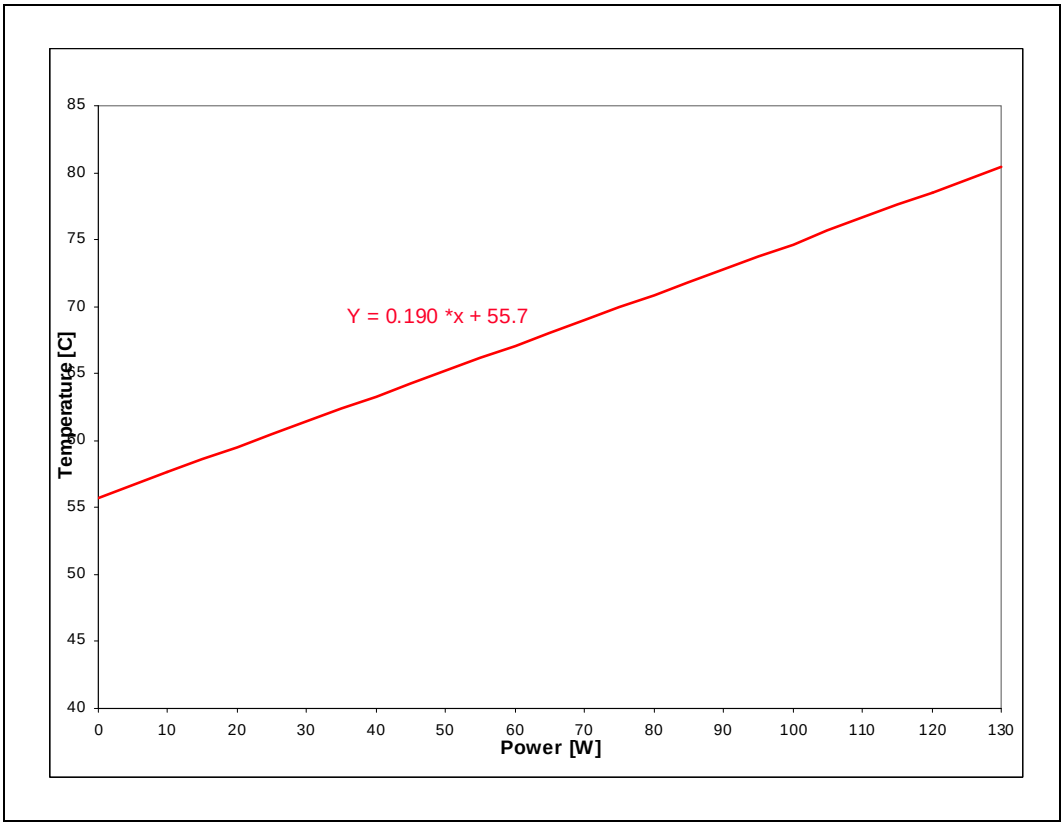
Notes:

1. The Frequency Optimized Server/Workstation Thermal Profile is representative of a volumetrically unconstrained platform. Please refer to Table 7-2 for discrete points that constitute the thermal profile.
2. Implementation of the Frequency Optimized Server/Workstation Processor Thermal Profile should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet the thermal profile will result in increased probability of TCC activation and may incur measurable performance loss.
3. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

Table 7-2. Frequency Optimized Server / Workstation Platform Thermal Profile (6 Core)

Power (W)	Maximum T_{CASE} (°C)
0	55.6
10	57.4
20	59.1
30	60.9
40	62.7
50	64.4
60	66.2
70	67.9
80	69.7
90	71.5
100	73.2
110	75.0
120	76.8
130	78.5

Figure 7-2. Frequency Optimized Server / Workstation Platform Thermal Profile (4 Core)



Notes:

1. The Frequency Optimized Server/Workstation Thermal Profile is representative of a volumetrically unconstrained platform. Please refer to Table 7-3 for discrete points that constitute the thermal profile.
2. Implementation of the Frequency Optimized Server/Workstation Processor Thermal Profile should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet the thermal profile will result in increased probability of TCC activation and may incur measurable performance loss.
3. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

Table 7-3. Frequency Optimized Server / Workstation Platform Thermal Profile (4 Core)

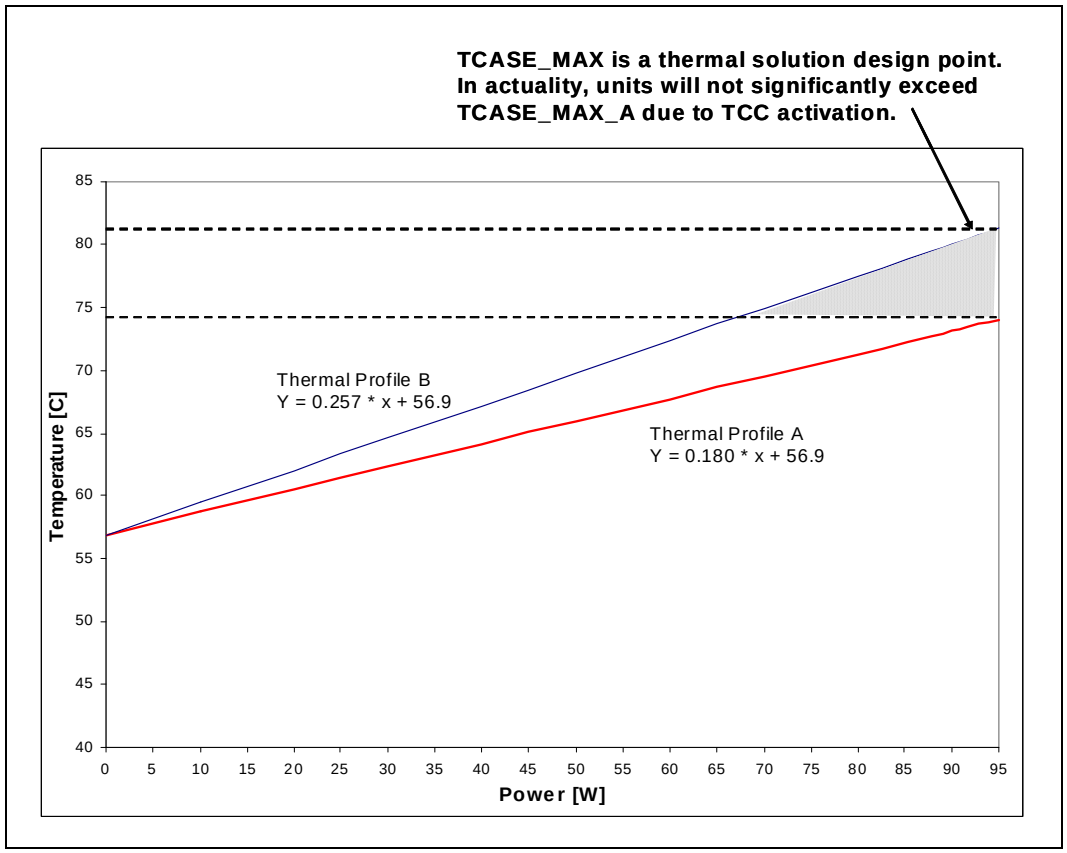
Power (W)	Maximum T_{CASE} (°C)
0	55.7
10	57.6
20	59.5
30	61.4
40	63.3
50	65.2
60	67.1
70	69.0
80	70.9
90	72.8
100	74.7
110	76.6
120	78.5
130	80.4

Table 7-4. Advanced Server / Workstation Platform Thermal Specifications

Core Frequency	Thermal Design Power (W)	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)	Notes
Launch to FMB	95	5	See Figure 7-3, Figure 7-4, Table 7-5, Table 7-6, Table 7-7, Table 7-8	1, 2, 3, 4

Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified ICC. Please refer to the electrical loadline specifications in Section 2.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. Power specifications are defined at all VIDs found in Table 2-2. Processors may be delivered under multiple VIDs for each frequency.
4. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 7-3. Advanced Server / Workstation Platform Thermal Profile A and B (6 Core)



Notes:
1. Thermal Profile A (refer to Table 7-5) is representative of a volumetrically unconstrained platform. Thermal Profile B (refer to Table 7-6) is representative of a volumetrically constrained platform.
2. Implementation of Thermal Profile A should result in virtually no TCC activation. Utilization of thermal solutions that do not meet Thermal Profile A will result in increased probability of TCC activation and may incur measurable performance loss.
3. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

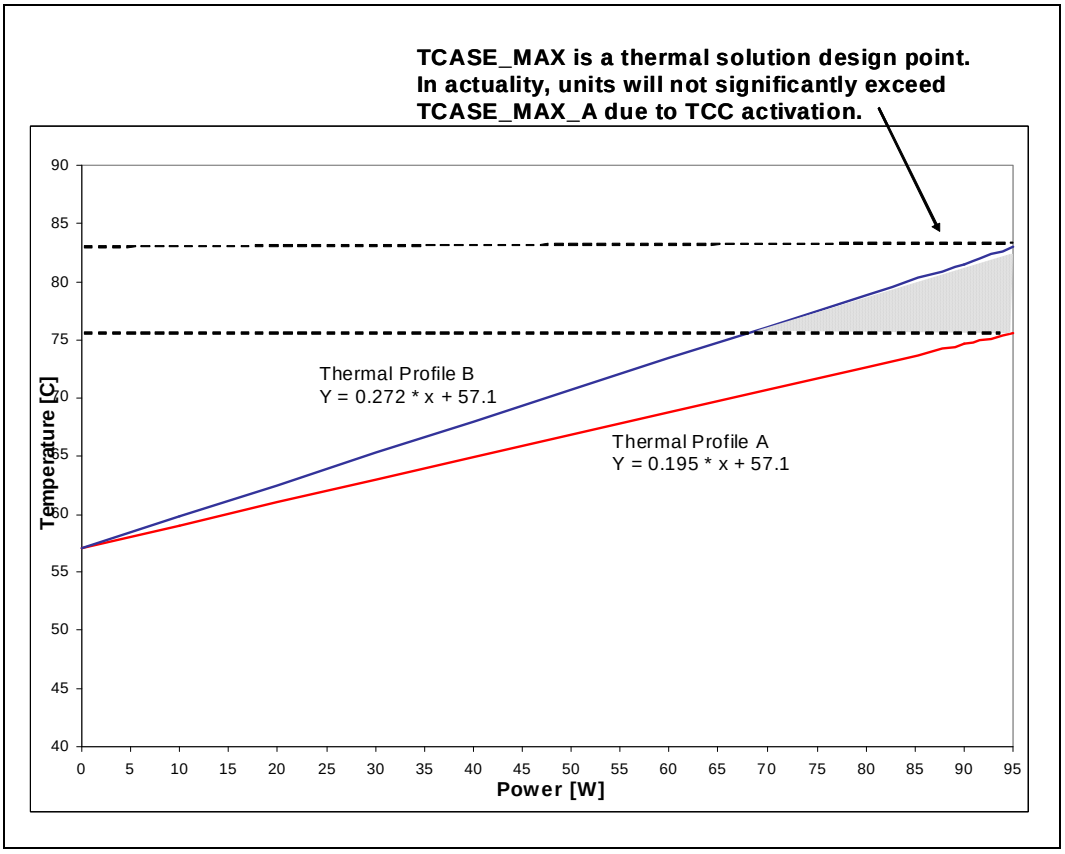
Table 7-5. Advanced Server / Workstation Thermal Profile A (6 Core)

Power (W)	Maximum T_{CASE} (°C)
0	56.9
10	58.7
20	60.5
30	62.3
40	64.1
50	65.9
60	67.7
70	69.5
80	71.3
90	73.1
95	74.0

Table 7-6. Advanced Server / Workstation Thermal Profile B (6 Core)

Power (W)	Maximum T_{CASE} (°C)
0	56.9
10	59.5
20	62.0
30	64.6
40	67.2
50	69.8
60	72.3
70	74.9
80	77.5
90	80.0
95	81.3

Figure 7-4. Advanced Server / Workstation Platform Thermal Profile A and B (4 Core)



Notes:

1. Thermal Profile A (refer to Table 7-7) is representative of a volumetrically unconstrained platform. Thermal Profile B (refer to Table 7-8) is representative of a volumetrically constrained platform.
2. Implementation of Thermal Profile A should result in virtually no TCC activation. Utilization of thermal solutions that do not meet Thermal Profile A will result in increased probability of TCC activation and may incur measurable performance loss.
3. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

Table 7-7. Advanced Server / Workstation Thermal Profile A (4 Core)

Power (W)	Maximum T_{CASE} (°C)
0	57.1
10	59.1
20	61.0
30	63.0
40	64.9
50	66.9
60	68.8
70	70.8
80	72.7
90	74.7
95	75.7

Table 7-8. Advanced Server/Workstation Thermal Profile B (4 Core)

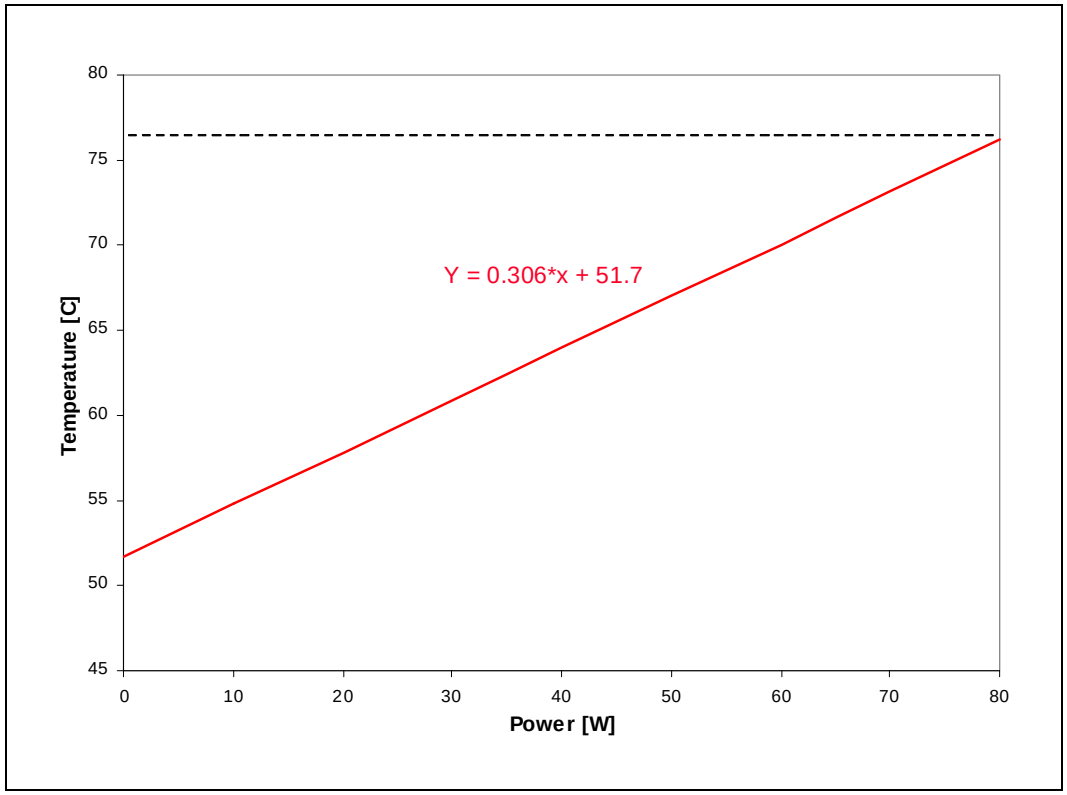
Power (W)	Maximum T_{CASE} (°C)
0	57.1
10	59.8
20	62.5
30	65.3
40	68.0
50	70.7
60	73.4
70	76.1
80	78.8
90	81.6
95	82.9

Table 7-9. Standard Server/Workstation Platform Thermal Specifications

Core Frequency	Thermal Design Power (W)	Minimum TCASE (°C)	Maximum TCASE (°C)	Notes
Launch to FMB	80	5	See Figure 7-5; Table 7-10, Figure 7-6, Table 7-11	1, 2, 3, 4

Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}. Please refer to the loadline specifications in Section 2.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. Power specifications are defined at all VIDs found in Table 2-2. The processor may be delivered under multiple VIDs for each frequency.
4. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 7-5. Standard Server / Workstation Platform Thermal Profile (6 Core)



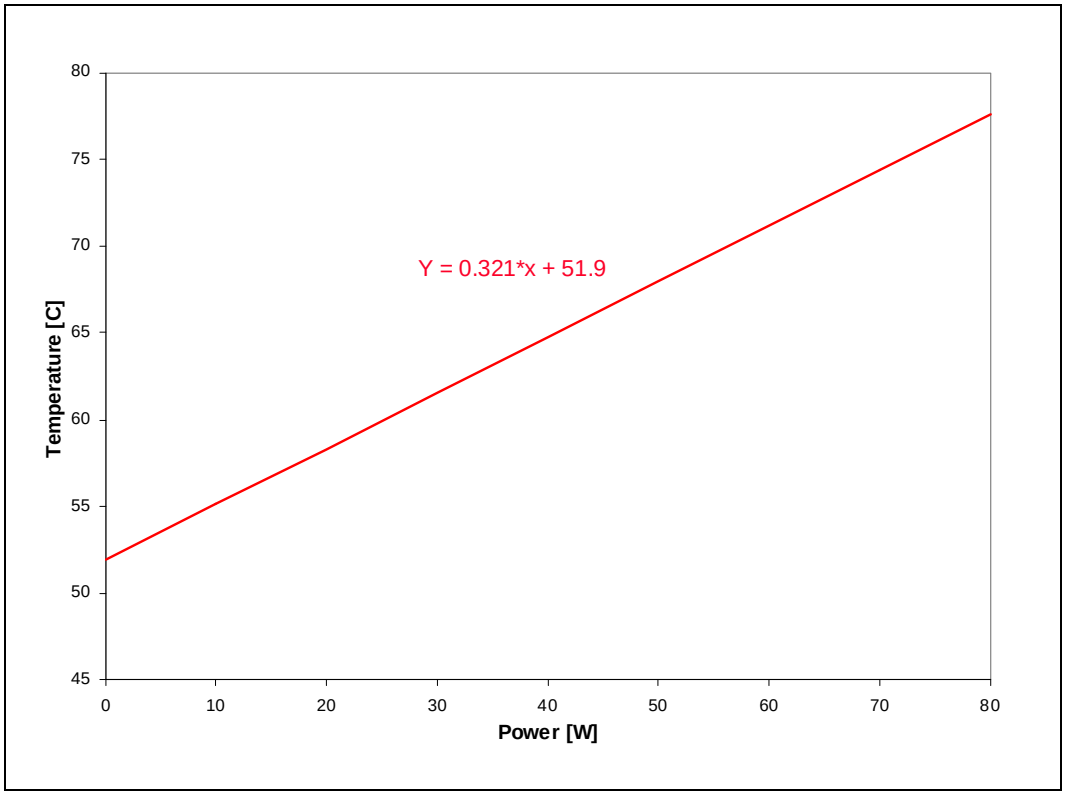
Notes:

1. The Thermal Profile is representative of a volumetrically constrained platform. Please refer to Table 7-10 for discrete points that constitute the thermal profile.
2. Implementation of the Thermal Profile should result in virtually no TCC activation. Utilization of thermal solutions that do not meet the Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss.
3. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

Table 7-10. Standard Server / Workstation Platform Thermal Profile (6 Core)

Power (W)	T_{CASE_MAX} (°C)
0	51.7
10	54.8
20	57.8
30	60.9
40	63.9
50	67.0
60	70.1
70	73.1
80	76.2

Figure 7-6. Standard Server / Workstation Platform Thermal Profile (4 Core)



Notes:

1. The Thermal Profile is representative of a volumetrically constrained platform. Please refer to Table 7-11 for discrete points that constitute the thermal profile.
2. Implementation of the Thermal Profile should result in virtually no TCC activation. Utilization of thermal solutions that do not meet the Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss.
3. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

Table 7-11. Standard Server / Workstation Platform Thermal Profile (4 Core)

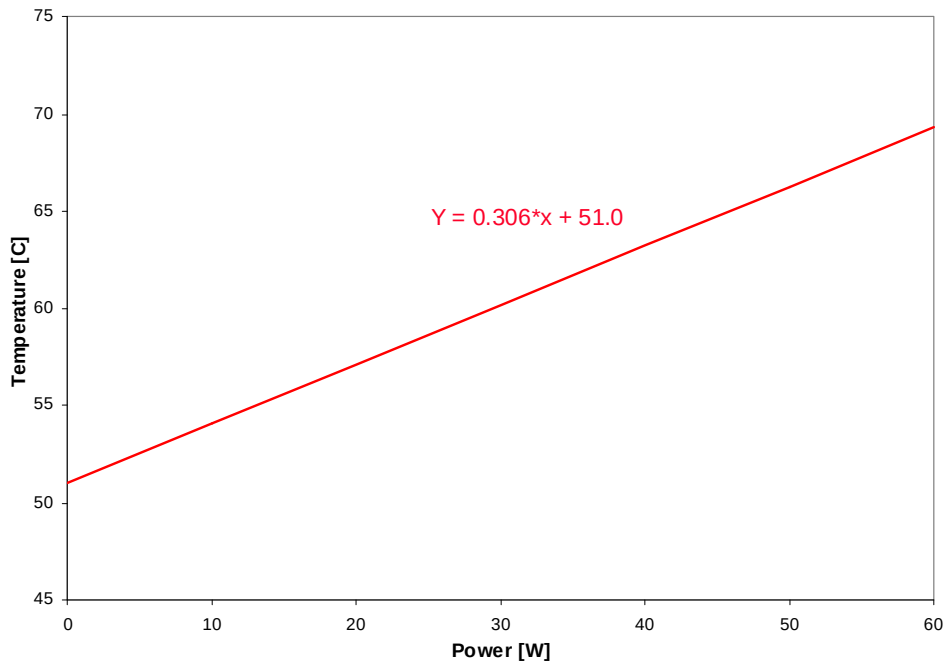
Power (W)	T_{CASE_MAX} (°C)
0	51.9
10	55.1
20	58.3
30	61.5
40	64.8
50	68.0
60	71.2
70	74.4
80	77.6

Table 7-12. Low Power Platform 60W Thermal Specifications

Core Frequency	Thermal Design Power (W)	Minimum TCASE (°C)	Maximum TCASE (°C)	Notes
Launch to FMB	60	5	See Figure 7-7; Table 7-13	1, 2, 3, 4

Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}. Please refer to the loadline specifications in Section 2.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. Power specifications are defined at all VIDs found in Table 2-2. The processor may be shipped under multiple VIDs for each frequency.
4. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 7-7. Low Power Platform 60W Thermal Profile (6 Core)



Notes:
1. The Thermal Profile is representative of a volumetrically constrained platform. Please refer to Table 7-13 for discrete points that constitute the thermal profile.
2. Implementation of the Thermal Profile should result in virtually no TCC activation. Utilization of thermal solutions that do not meet the Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss.
3. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

Table 7-13. Low Power Platform 60W Thermal Profile (6 Core) (Sheet 1 of 2)

Power (W)	Maximum T_{CASE} (°C)
0	51.0
10	54.0
20	57.1

Table 7-13. Low Power Platform 60W Thermal Profile (6 Core) (Sheet 2 of 2)

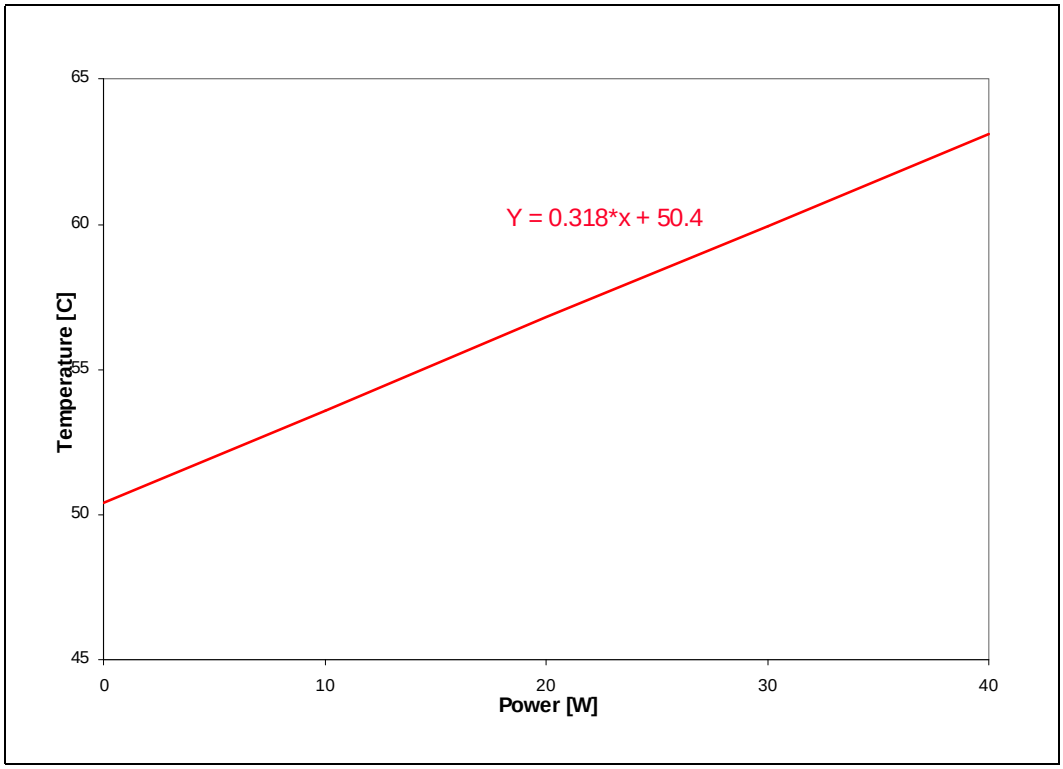
Power (W)	Maximum T_{CASE} (°C)
30	60.2
40	63.2
50	66.3
60	69.4

Table 7-14. Low Power Platform 40W Thermal Specifications

Core Frequency	Thermal Design Power (W)	Minimum TCASE (°C)	Maximum TCASE (°C)	Notes
Launch to FMB	40	5	See Figure 7-8; Table 7-15	1, 2, 3, 4

Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}. Please refer to the loadline specifications in Section 2.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. Power specifications are defined at all VIDs found in Table 2-2. The processor may be shipped under multiple VIDs for each frequency.
4. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 7-8. Low Power Platform 40W Thermal Profile (4 Core)



Notes:
1. The Thermal Profile is representative of a volumetrically constrained platform. Please refer to Table 7-15 for discrete points that constitute the thermal profile.
2. Implementation of the Thermal Profile should result in virtually no TCC activation. Utilization of thermal solutions that do not meet the Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss.

3. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

Table 7-15. Low Power Platform 40W Thermal Profile (4 Core)

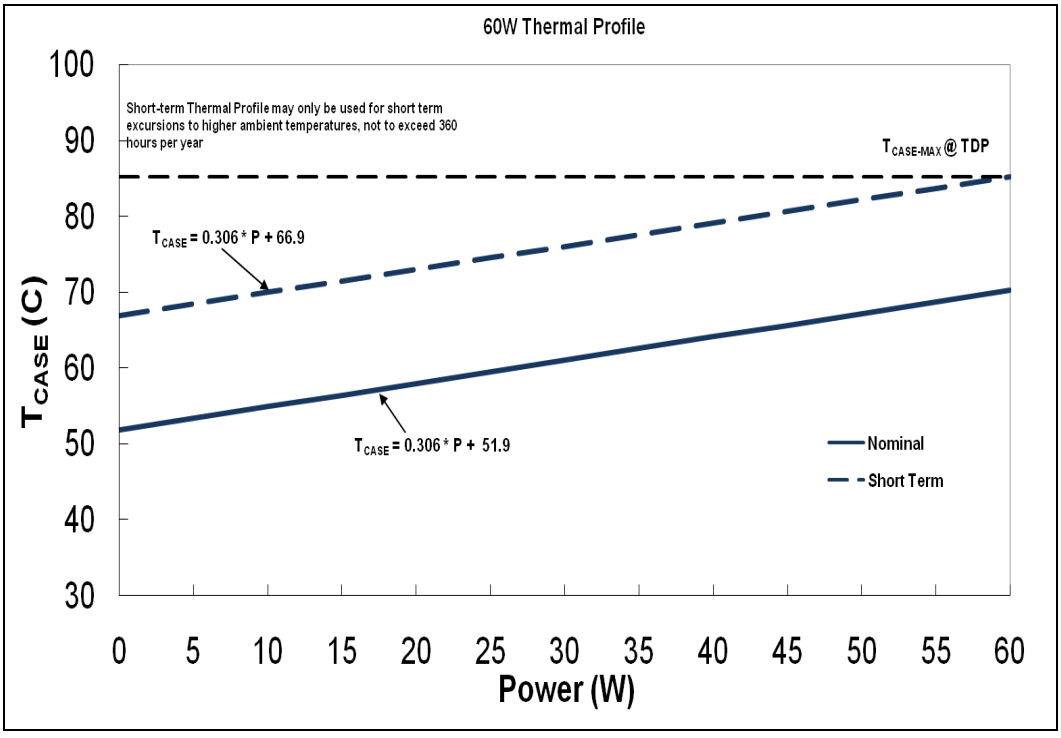
Power (W)	Maximum T_{CASE} (°C)
0	50.4
10	53.6
20	56.8
30	59.9
40	63.1

Table 7-16. LV-60W Processor Thermal Specifications

Core Frequency	Thermal Design Power (W)	Minimum TCASE (°C)	Maximum TCASE (°C)	Notes
Launch to FMB	60	5	See Figure 7-9; Table 7-17	1, 2, 3, 4

Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}. Please refer to the loadline specifications in Section 2.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. Power specifications are defined at all VIDs found in Table 2-2. The processor may be shipped under multiple VIDs for each frequency.
4. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 7-9. LV-60W Processor Dual Thermal Profile



Notes:
1. The Thermal Profile is representative of a volumetrically constrained platform. Please refer to Table 7-17 for discrete points that constitute the thermal profile.

2. Implementation of the nominal and short-term Thermal Profiles should result in virtually no TCC activation. Utilization of thermal solutions that do not meet the Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss.
3. The Nominal Thermal Profile must be used for all normal operating conditions, or for products that do not require NEBS Level 3 compliance.
4. The Short-Term Thermal Profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 96 hours per instance, 360 hours per year, and a maximum of 15 instances per year, as compliant with NEBS Level 3. Operation at the Short-Term Thermal Profile for durations exceeding 360 hours per year violate the processor thermal specifications and may result in permanent damage to the processor.
5. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

Table 7-17. LV-60W Processor Dual Thermal Profile

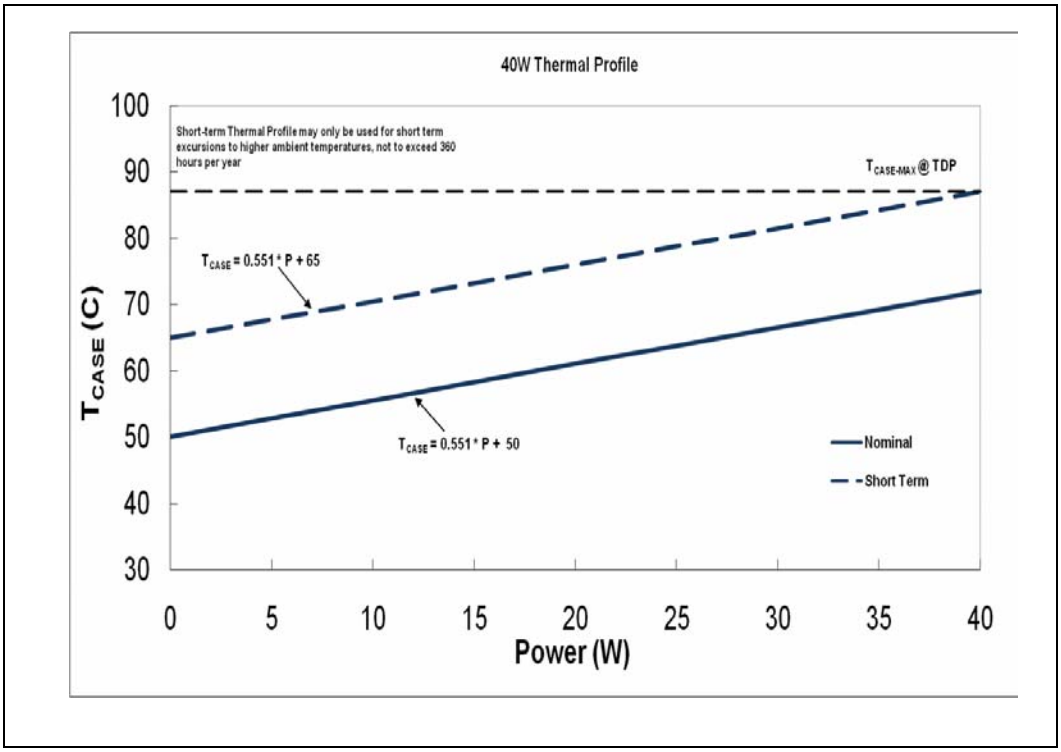
Power (W)	Nominal T_{CASE_MAX} (°C)	Maximum T_{CASE_MAX} (°C)
0	52	67
10	55	70
20	58	73
30	61	76
40	64	79
50	67	82
60	70	85

Table 7-18. LV-40W Processor Thermal Specifications

Core Frequency	Thermal Design Power (W)	Minimum TCASE (°C)	Maximum TCASE (°C)	Notes
Launch to FMB	40	5	See Figure 7-10; Table 7-19	1, 2, 3, 4

Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}. Please refer to the loadline specifications in Section 2.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. Power specifications are defined at all VIDs found in Table 2-2. The processor may be shipped under multiple VIDs for each frequency.
4. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 7-10. LV-40W Processor Dual Thermal Profile



Notes:

1. The Thermal Profile is representative of a volumetrically constrained platform. Please refer to Table 7-19 for discrete points that constitute the thermal profile.
2. Implementation of the nominal and short-term Thermal Profiles should result in virtually no TCC activation. Utilization of thermal solutions that do not meet the Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss.
3. The Nominal Thermal Profile must be used for all normal operating conditions, or for products that do not require NEBS Level 3 compliance.
4. The Short-Term Thermal Profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 96 hours per instance, 360 hours per year, and a maximum of 15 instances per year, as compliant with NEBS Level 3. Operation at the Short-Term Thermal Profile for durations exceeding 360 hours per year violate the processor thermal specifications and may result in permanent damage to the processor.
5. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

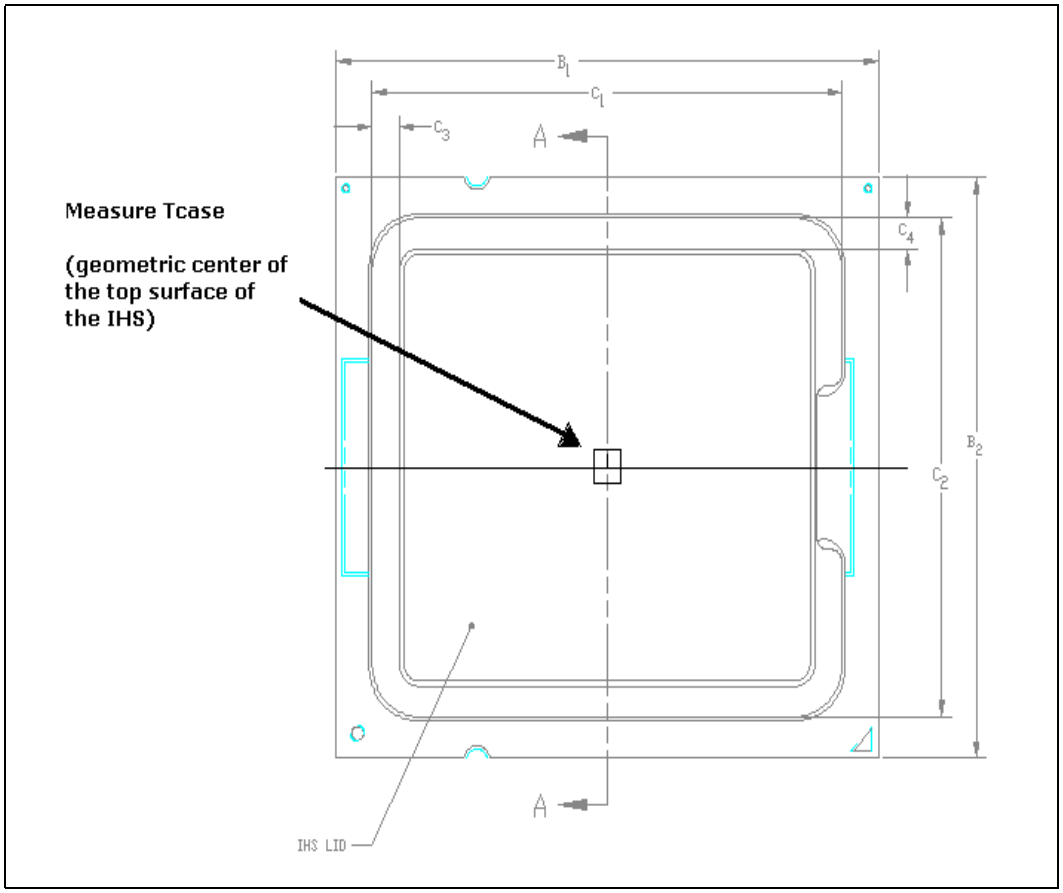
Table 7-19. LV-40W Processor Dual Thermal Profile

Power (W)	Nominal T_{CASE_MAX} (°C)	Short-term T_{CASE_MAX} (°C)
0	50	65
5	53	68
10	56	71
15	58	73
20	61	76
25	64	79
30	67	82
35	69	84
40	72	87

7.1.2 Thermal Metrology

The minimum and maximum case temperatures (T_{CASE}) are specified in Table 7-1,Table 7-4, Table 7-9. Table 7-12, Table 7-14, Table 7-16 and Table 7-18 and are measured at the geometric top center of the processor integrated heat spreader (IHS). Figure 7-11 illustrates the location where T_{CASE} temperature measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines*.

Figure 7-11. Case Temperature (T_{CASE}) Measurement Location

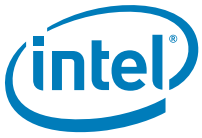


Notes:
1. Figure is not to scale and is for reference only.
2. B1: Max = 45.07 mm, Min = 44.93 mm.
3. B2: Max = 42.57 mm, Min = 42.43 mm.
4. C1: Max = 39.1 mm, Min = 38.9 mm.
5. C2: Max = 36.6 mm, Min = 36.4 mm.
6. C3: Max = 2.3 mm, Min = 2.2 mm
7. C4: Max = 2.3 mm, Min = 2.2 mm.

7.2 Processor Thermal Features

7.2.1 Processor Temperature

A new feature in the Intel Xeon processor 5600 series is a software readable field in the IA32_TEMPERATURE_TARGET register that contains the minimum temperature at which the TCC will be activated and PROCHOT# will be asserted. The TCC activation



temperature is calibrated on a part-by-part basis and normal factory variation may result in the actual TCC activation temperature being higher than the value listed in the register. TCC activation temperatures may change based on processor stepping, frequency or manufacturing efficiencies.

NOTE: There is no specified correlation between DTS temperatures and processor case temperatures; therefore it is not possible to use this feature to ensure the processor case temperature meets the Thermal Profile specifications.

7.2.2 Adaptive Thermal Monitor

The Adaptive Thermal Monitor feature provides an enhanced method for controlling the processor temperature when the processor silicon reaches its maximum operating temperature. Adaptive Thermal Monitor uses Thermal Control Circuit (TCC) activation to reduce processor power via a combination of methods. The first method (Frequency/VID control) involves the processor adjusting its operating frequency (via the core ratio multiplier) and input voltage (via the VID signals). This combination of reduced frequency and VID results in a reduction to the processor power consumption. The second method (clock modulation) reduces power consumption by modulating (starting and stopping) the internal processor core clocks. The processor intelligently selects the appropriate TCC method to use on a dynamic basis. BIOS is not required to select a specific method (as with previous-generation processors supporting TM1 or TM2).

The Adaptive Thermal Monitor feature must be enabled for the processor to be operating within specifications. The temperature at which Adaptive Thermal Monitor activates the Thermal Control Circuit is not user configurable and is not software visible. Snooping and interrupt processing are performed in the normal manner while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and in some cases may result in a T_C that exceeds the specified maximum temperature which may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines* for information on designing a compliant thermal solution.

The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and cannot be modified. The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

7.2.2.1 Frequency/VID Control

The processor uses Frequency/VID control whereby TCC activation causes the processor to adjust its operating frequency (via the core ratio multiplier) and input voltage (via the VID signals). This combination of reduced frequency and VID results in a reduction to the processor power consumption.

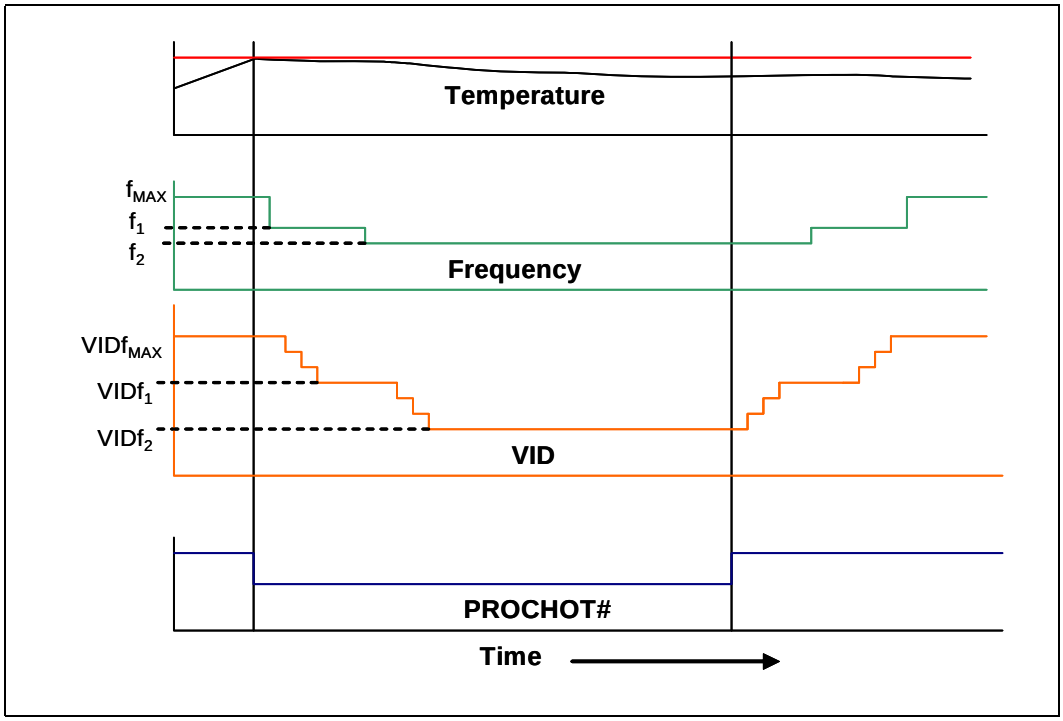
This method includes multiple operating points, each consisting of a specific operating frequency and voltage. The first operating point represents the normal operating condition for the processor. The remaining points consist of both lower operating

frequencies and voltages. When the TCC is activated, the processor automatically transitions to the new operating frequency. This transition occurs very rapidly (on the order of 2 µs).

Once the new operating frequency is engaged, the processor will transition to the new core operating voltage by issuing a new VID code to the voltage regulator. The voltage regulator must support dynamic VID steps to support this method. During the voltage change, it will be necessary to transition through multiple VID codes to reach the target operating voltage. Each step will be one VID table entry (see Table 2-2). The processor continues to execute instructions during the voltage transition. Operation at the lower voltages reduces the power consumption of the processor.

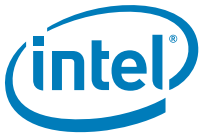
A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the operating frequency and voltage transition back to the normal system operating point via the intermediate VID/frequency points. Transition of the VID code will occur first, to insure proper operation once the processor reaches its normal operating frequency. Refer to Figure 7-12 for an illustration of this ordering.

Figure 7-12. Frequency and Voltage Ordering



7.2.2.2 Clock Modulation

Clock modulation is performed by alternately turning the clocks off and on at a duty cycle specific to the processor (factory configured to 37.5% on and 62.5% off for TM1). The period of the duty cycle is configured to 32 microseconds when the TCC is active. Cycle times are independent of processor frequency. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases. Clock



modulation is automatically engaged as part of the TCC activation when the Frequency/VID targets are at their minimum settings. It may also be initiated by software at a configurable duty cycle.

7.2.3 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as “On-Demand” mode and is distinct from the Adaptive Thermal Monitor feature. On-Demand mode is intended as a means to reduce system level power consumption. Systems must not rely on software usage of this mechanism to limit the processor temperature. If bit 4 of the IA32_CLOCK_MODULATION MSR is set to a ‘1’, the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same IA32_CLOCK_MODULATION MSR. In On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used in conjunction with the Adaptive Thermal Monitor; however, if the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

7.2.4 PROCHOT# Signal

An external signal, PROCHOT# (processor hot), is asserted when the processor core temperature has reached its maximum operating temperature. If Adaptive Thermal Monitor is enabled (note it must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#.

The PROCHOT# signal is bi-directional in that it can either signal when the processor (any core) has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

As an output, PROCHOT# will go active when the processor temperature monitoring sensor detects that one or more cores has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled, for all cores. TCC activation due to PROCHOT# assertion by the system will result in the processor immediately transitioning to the minimum frequency and corresponding voltage (using Freq/VID control). Clock modulation is not activated in this case. The TCC will remain active until the system de-asserts PROCHOT#.

PROCHOT# can allow voltage regulator (VR) thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its Thermal Design Power.

With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# will only be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

7.2.5 THERMTRIP# Signal

Regardless of whether Adaptive Thermal Monitor is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (refer to the THERMTRIP# definition in Table 6-1). At this point, the THERMTRIP# signal will go active and stay active. THERMTRIP# activation is independent of processor activity and does not generate any Intel® QuickPath Interconnect transactions. If THERMTRIP# is asserted, processor V_{CC} and V_{TT} must be removed within the timeframe defined in Table 2-26. The temperature at which THERMTRIP# asserts is not user configurable and is not software visible.

7.3 Platform Environment Control Interface (PECI)

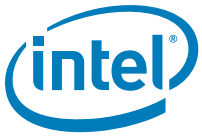
The Platform Environment Control Interface (PECI) uses a single wire for self-clocking and data transfer. The bus requires no additional control lines. The physical layer is a self-clocked one-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a logic ‘0’ or logic ‘1’. PECI also includes variable data transfer rate established with every message. In this way, it is highly flexible even though underlying logic is simple.

The interface design was optimized for interfacing to Intel processor and chipset components in both single processor and multiple processor environments. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information.

The PECI bus offers:

- A wide speed range from 2 kbps to 2 Mbps
- CRC check byte used to efficiently and atomically confirm accurate data delivery
- Synchronization at the beginning of every message minimizes device timing accuracy requirements

Intel recommends PECI host device speeds of 1.2 Mbps or lower for platforms using the Intel Xeon processor 5600 series. PECI host devices operating at speeds greater than 1.2 Mbps may get a CPU “Timeout” error response to the PCI-ConfigRd() and PCIConfigWr() PECI commands. This is expected to happen only during the deepest idle states on Intel Xeon processor 5600 series. If higher bit rates are required, platforms must be tolerant of “Timeout” completion codes during the deepest processor package C-states. Please note that processors always request a 2 Mbps bit rate, and



will accept lower bit rates from a host according to timing negotiation specifications. What follows is a processor-specific PECI client definition. PECI commands listed in Table 7-20 apply to Intel Xeon processor 5600 series only.

Table 7-20. Summary of Processor-Specific PECI Commands

Command	Intel® Xeon® Processor 5600 Series Support
Ping()	Yes
GetDIB()	Yes
GetTemp()	Yes
PCIConfigRd()	Yes
PCIConfigWr()	Yes
MbxSend() [1]	Yes
MbxGet() [1]	Yes

Note:
1. Refer to Table 7-25 for a summary of mailbox commands supported by the Intel Xeon processor 5600 series.

7.3.1 PECI Client Capabilities

Intel Xeon processor 5600 series acting as PECI clients support the following sideband functions:

- Processor and DRAM thermal management
- Platform manageability functions including thermal, power and electrical error monitoring
- Processor interface tuning and diagnostics capabilities (Intel® IBIST).

7.3.1.1 Thermal Management

Processor fan speed control is managed by comparing PECI thermal readings against the processor-specific fan speed control reference point, or $T_{CONTROL}$. Both $T_{CONTROL}$ and PECI thermal readings are accessible via the processor PECI client. These variables are referenced to a common temperature, the TCC activation point, and are both defined as negative offsets from that reference.

PECI-based access to DRAM thermal readings and throttling control coefficients provide a means for Board Management Controllers (BMCs) or other platform management devices to feed hints into on-die memory controller throttling algorithms. These control coefficients are accessible using PCI configuration space writes via PECI. The PECI-based configuration write functionality is defined in Section 7.3.2.5, and the DRAM throttling coefficient control functions are documented in the *Intel® Xeon® Processor 5600 Series Datasheet, Volume 2*.

7.3.1.2 Platform Manageability

PECI allows full read access to error and status monitoring registers within the processor's PCI configuration space. It also provides insight into thermal monitoring functions such as TCC activation timers and thermal error logs.

The exact list of RAS-related registers in the PCI configuration space can be found in the *Intel® Xeon® Processor 5600 Series Datasheet, Volume 2*.

7.3.1.3 Processor Interface Tuning and Diagnostics

Intel Xeon processor 5600 series Intel IBIST allows for in-field diagnostic capabilities in Intel® QuickPath Interconnect and memory controller interfaces. PECI provides a port to execute these diagnostics via its PCI Configuration read and write capabilities.

7.3.2 Client Command Suite

7.3.2.1 Ping()

Ping() is a required message for all PECI devices. This message is used to enumerate devices or determine if a device has been removed, been powered-off, etc. A Ping() sent to a device address always returns a non-zero Write FCS if the device at the targeted address is able to respond.

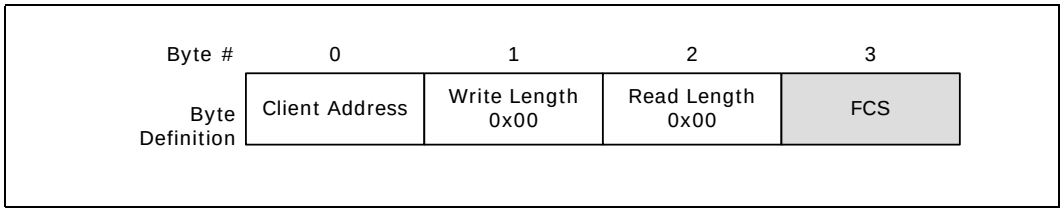
7.3.2.1.1 Command Format

The Ping() format is as follows:

Write Length: 0

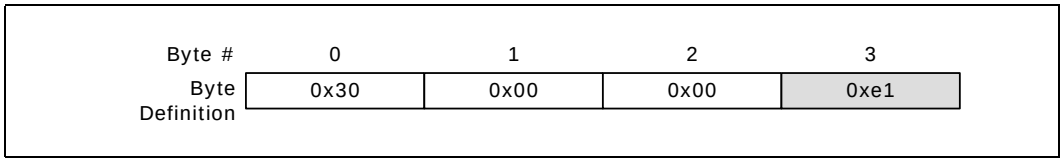
Read Length: 0

Figure 7-13. Ping()



An example Ping() command to PECI device address 0x30 is shown below.

Figure 7-14. Ping() Example



7.3.2.2 GetDIB()

The processor PECI client implementation of GetDIB() includes an 8-byte response and provides information regarding client revision number and the number of supported domains. All processor PECI clients support the GetDIB() command.

7.3.2.2.1 Command Format

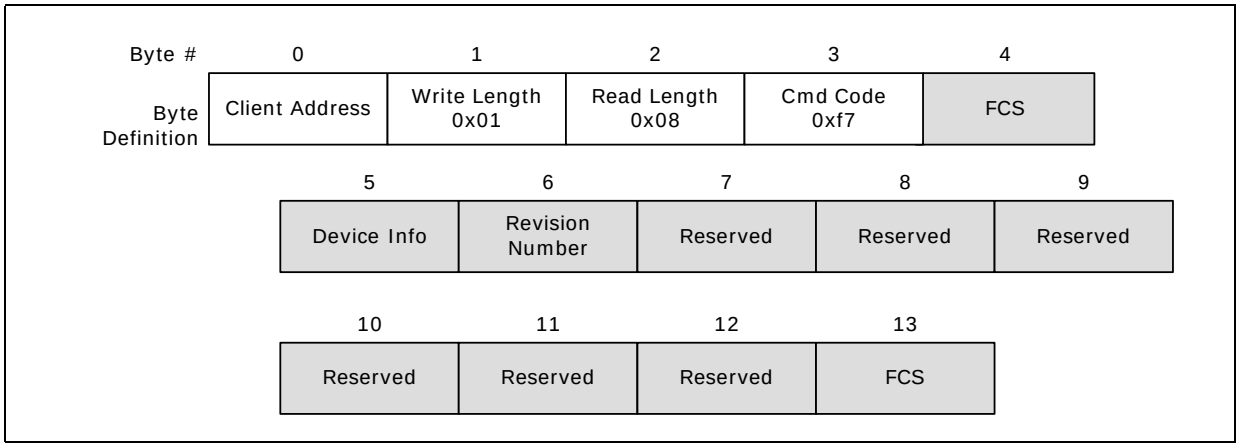
The GetDIB() format is as follows:

Write Length: 1

Read Length: 8

Command: 0xf7

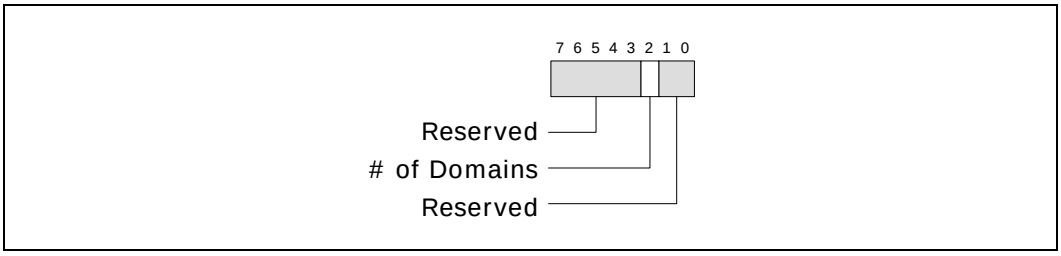
Figure 7-15. GetDIB()



7.3.2.2.2 Device Info

The Device Info byte gives details regarding the PECI client configuration. At a minimum, all clients supporting GetDIB will return the number of domains inside the package via this field. With any client, at least one domain (Domain 0) must exist. Therefore, the Number of Domains reported is defined as the number of domains in addition to Domain 0. For example, if the number 0b1 is returned, that would indicate that the PECI client supports two domains.

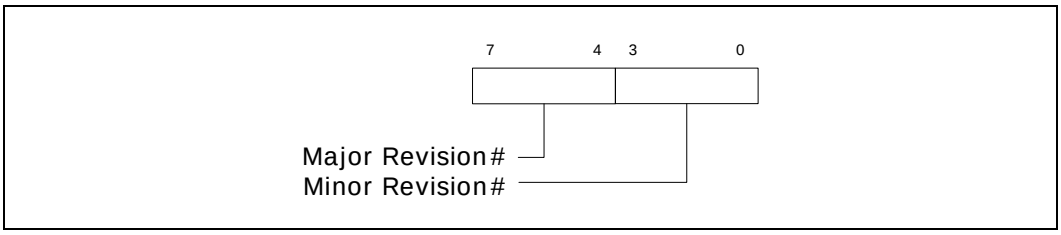
Figure 7-16. Device Info Field Definition



7.3.2.2.3 Revision Number

All clients that support the GetDIB command also support Revision Number reporting. The revision number may be used by a host or originator to manage different command suites or response codes from the client. Revision Number is always reported in the second byte of the GetDIB() response. The Revision Number always maps to the revision number of this document.

Figure 7-17. Revision Number Definition



For a client that is designed to meet the PECI Specification, it returns '0010 0000b'.

7.3.2.3 GetTemp()

The GetTemp() command is used to retrieve the temperature from a target PECI address. The temperature is used by the external thermal management system to regulate the temperature on the die. The data is returned as a negative value representing the number of degrees centigrade below the Thermal Control Circuit Activation temperature of the PECI device. Note that a value of zero represents the temperature at which the Thermal Control Circuit activates. The actual value that the thermal management system uses as a control set point (Tcontrol) is also defined as a negative number below the Thermal Control Circuit Activation temperature. TCONTROL may be extracted from the processor by issuing a PECI Mailbox MbxGet() (see Section 7.3.2.8), or using a RDMSR instruction.

Please refer to Section 7.3.6 for details regarding temperature data formatting.

7.3.2.3.1 Command Format

The GetTemp() format is as follows:

Write Length: 1

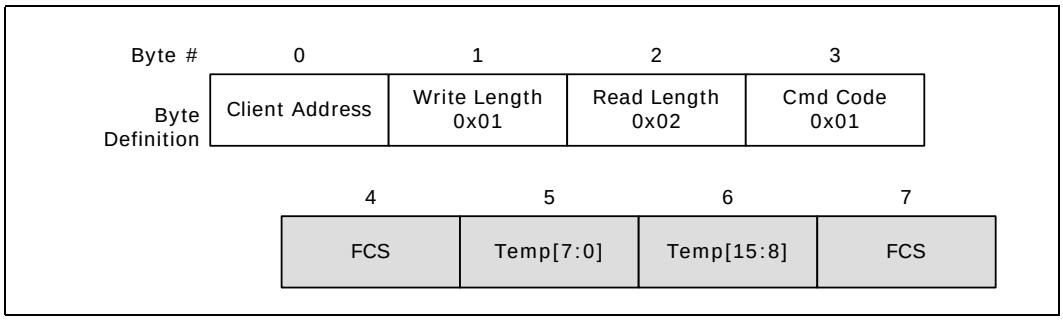
Read Length: 2

Command: 0x01

Multi-Domain Support: Yes (see Table 7-32)

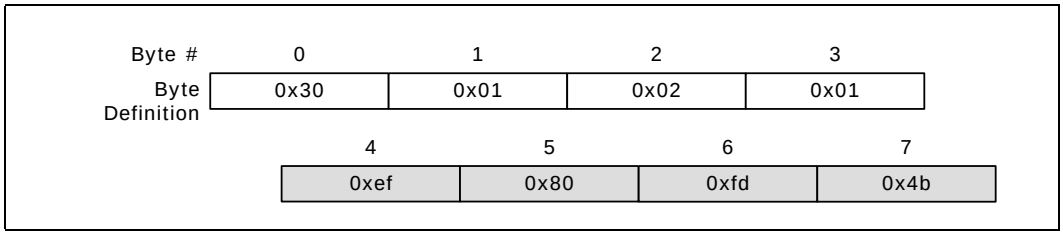
Description: Returns the current temperature for addressed processor PECI client.

Figure 7-18. GetTemp()



Example bus transaction for a thermal sensor device located at address 0x30 returning a value of negative 10° C:

Figure 7-19. GetTemp() Example



7.3.2.3.2 Supported Responses

The typical client response is a passing FCS and good thermal data. Under some conditions, the client's response will indicate a failure.

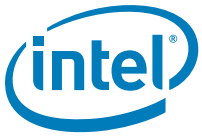


Table 7-21. GetTemp() Response Definition

Response	Meaning
General Sensor Error (GSE)	Thermal scan did not complete in time. Retry is appropriate.
0x0000	Processor is running at its maximum temperature or is currently being reset.
All other data	Valid temperature reading, reported as a negative offset from the TCC activation temperature.

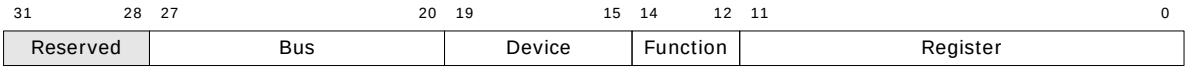
7.3.2.4 PCIConfigRd()

The PCIConfigRd() command gives sideband read access to the entire PCI configuration space maintained in the processor. This capability does not include support for route-through to downstream devices or sibling processors. The exact listing of supported devices, functions, and registers can be found in the *Intel® Xeon® Processor 5600 Series Datasheet, Volume 2*. PECI originators may conduct a device/function/register enumeration sweep of this space by issuing reads in the same manner that BIOS would. A response of all 1's indicates that the device/function/register is unimplemented.

PCI configuration addresses are constructed as shown in the following diagram. Under normal in-band procedures, the Bus number (including any reserved bits) would be used to direct a read or write to the proper device. Since there is a one-to-one mapping between any given client address and the bus number, any request made with a non-zero Bus number is ignored and the client will respond with a 'pass' completion code but all 0's in the data. The only legal bus number is 0x00. The client will return all 1's in the data response and 'pass' for the completion code for all of the following conditions:

- Unimplemented Device
- Unimplemented Function
- Unimplemented Register

Figure 7-20. PCI Configuration Address



PCI configuration reads may be issued in byte, word, or dword granularities.

7.3.2.4.1 Command Format

The PCIConfigRd() format is as follows:

Write Length: 5

Read Length: 2 (byte data), 3 (word data), 5 (dword data)

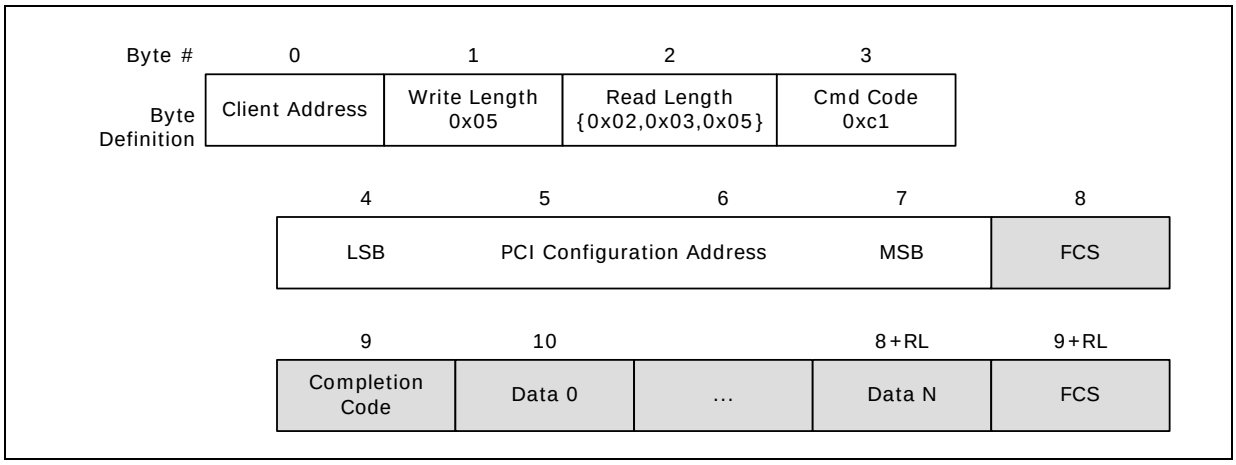
Command: 0xc1

Multi-Domain Support: Yes (see Table 7-32)

Description: Returns the data maintained in the PCI configuration space at the PCI configuration address sent. The Read Length dictates the desired data return size. This command supports byte, word, and dword responses as well as a completion code. All

command responses are prepended with a completion code that includes additional pass/fail status information. Refer to Section 7.3.4.2 for details regarding completion codes.

Figure 7-21. PCIConfigRd()



Note that the 4-byte PCI configuration address defined above is sent in standard PECI ordering with LSB first and MSB last.

7.3.2.4.2 Supported Responses

The typical client response is a passing FCS, a passing Completion Code (CC) and valid Data. Under some conditions, the client's response will indicate a failure.

Table 7-22. PCIConfigRd() Response Definition

Response	Meaning
Abort FCS	Illegal command formatting (mismatched RL/WL/Command Code)
CC: 0x40	Command passed, data is valid
CC: 0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET or processor S1 state. Retry is appropriate outside of the RESET or S1 states.

7.3.2.5 PCIConfigWr()

The PCIConfigWr() command gives sideband write access to the PCI configuration space maintained in the processor. The exact listing of supported devices, functions is defined below in Table 7-23. PECI originators may conduct a device/function/register enumeration sweep of this space by issuing reads in the same manner that BIOS would.

Table 7-23. PCIConfigWr() Device/Function Support (Sheet 1 of 2)

Writable		Description
Device	Function	
2	1	Intel® QuickPath Interconnect Link 0 Intel IBIST
2	5	Intel® QuickPath Interconnect Link 1 Intel IBIST
3	4	Memory Controller Intel IBIST[1]

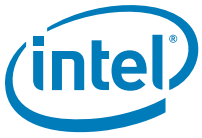


Table 7-23. PCIConfigWr() Device/Function Support (Sheet 2 of 2)

Writable		Description
Device	Function	
4	3	Memory Controller Channel 0 Thermal Control / Status
5	3	Memory Controller Channel 1 Thermal Control / Status
6	3	Memory Controller Channel 2 Thermal Control / Status

Note:
1. Currently not available for access through the PECI PCIConfigWr() command.

PCI configuration addresses are constructed as shown in Figure 7-20, and this command is subject to the same address configuration rules as defined in Section 7.3.2.4. PCI configuration reads may be issued in byte, word, or dword granularities.

Because a PCIConfigWr() results in an update to potentially critical registers inside the processor, it includes an Assured Write FCS (AW FCS) byte as part of the write data payload. In the event that the AW FCS mismatches with the client-calculated FCS, the client will abort the write and will always respond with a bad Write FCS.

7.3.2.5.1 Command Format

The PCIConfigWr() format is as follows:

Write Length: 7 (byte), 8 (word), 10 (dword)

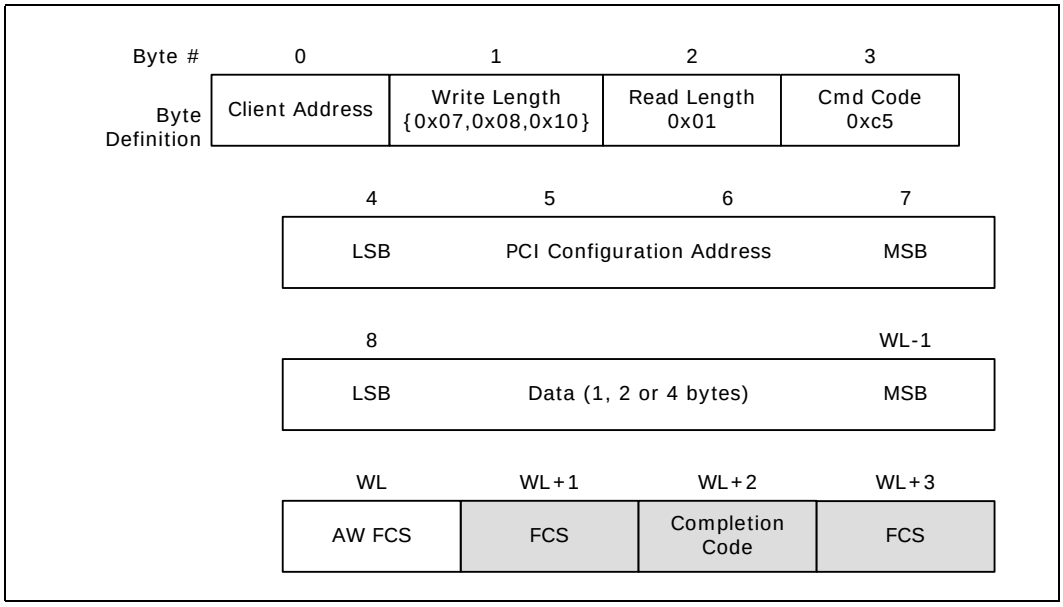
Read Length: 1

Command: 0xc5

Multi-Domain Support: Yes (see Table 7-32)

Description: Writes the data sent to the requested register address. Write Length dictates the desired write granularity. The command always returns a completion code indicating the pass/fail status information. Write commands issued to illegal (non-zero) Bus Numbers, or unimplemented Device / Function / Register addresses are ignored but return a passing completion code. Refer to Section 7.3.4.2 for details regarding completion codes.

Figure 7-22. PCIConfigWr()



Note that the 4-byte PCI configuration address and data defined above are sent in standard PECI ordering with LSB first and MSB last.

7.3.2.5.2 Supported Responses

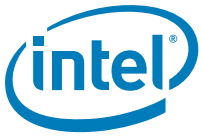
The typical client response is a passing FCS, a passing Completion Code and valid Data. Under some conditions, the client's response will indicate a failure.

Table 7-24. PCIConfigWr() Response Definition

Response	Meaning
Bad FCS	Electrical error or AW FCS failure
Abort FCS	Illegal command formatting (mismatched RL/WL/Command Code)
CC: 0x40	Command passed, data is valid
CC: 0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET condition or processor S1 state. Retry is appropriate outside of the RESET or S1 states.

7.3.2.6 Mailbox

The PECI mailbox ("Mbx") is a generic interface to access a wide variety of internal processor states. A Mailbox request consists of sending a 1-byte request type and 4-byte data to the processor, followed by a 4-byte read of the response data. The following sections describe the Mailbox capabilities as well as the usage semantics for the MbxSend and MbxGet commands which are used to send and receive data.



7.3.2.6.1 Capabilities

Table 7-25. Mailbox Command Summary

Command Name	Request Type Code (byte)	MbxSend Data (dword)	MbxGet Data (dword)	Description
Ping	0x00	0x00	0x00	Verify the operability / existence of the Mailbox.
Thermal Status Read/Clear	0x01	Log bit clear mask	Thermal Status Register	Read the thermal status register and optionally clear any log bits. The thermal status has status and log bits indicating the state of processor TCC activation, external PROCHOT# assertion, and Critical Temperature threshold crossings.
Counter Snapshot	0x03	0x00	0x00	Snapshots all PECI-based counters
Counter Clear	0x04	0x00	0x00	Concurrently clear and restart all counters.
Counter Read	0x05	Counter Number	Counter Data	Returns the counter number requested. 0: Total reference time 1: Total TCC Activation time counter
Icc-TDC Read	0x06	0x00	Icc-TDC	Returns the specified Icc-TDC of this part, in Amps.
Thermal Config Data Read	0x07	0x00	Thermal config data	Reads the thermal averaging constant.
Thermal Config Data Write	0x08	Thermal Config Data	0x00	Writes the thermal averaging constant.
Tcontrol Read	0x09	0x00	Tcontrol	Reads the fan speed control reference temperature, Tcontrol, in PECI temperature format.
Machine Check Read	0x0A	Bank Number / Index	Register Data	Read processor Machine Check Banks.
T-State Throttling Control Read	0x0B	0x00	ACPI T-state Control Word	Reads the PECI ACPI T-state throttling control word.
T-State Throttling Control Write	0x0C	ACPI T-state Control Word	0x00	Writes the PECI ACPI T-state throttling control word.
Read Energy Accumulator	0x0F	0x00	Energy Data	Reads processor energy accumulator

Any MbxSend request with a request type not defined in Table 7-25 will result in a failing completion code.

7.3.2.6.2 Ping

The Mailbox interface may be checked by issuing a Mailbox 'Ping' command. If the command returns a passing completion code, it is functional. Under normal operating conditions, the Mailbox Ping command should always pass.

7.3.2.6.3 Thermal Status Read / Clear

The Thermal Status Read provides information on package level thermal status. Data includes:

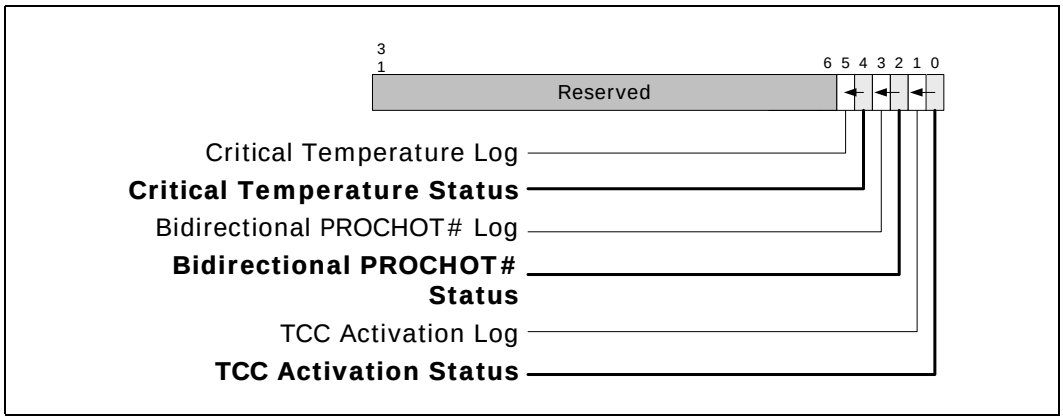
- The status of TCC activation
- Bidirectional PROCHOT# assertion
- Critical Temperature

These status bits are a subset of the bits defined in the IA32_THERM_STATUS MSR on the processor, and more details on the meaning of these bits may be found in the *Intel® 64 and IA-32 Architectures Software Developer's Manual*, Vol 3B.

Both status and sticky log bits are managed in this status word. All sticky log bits are set upon a rising edge of the associated status bit, and the log bits are cleared only by Thermal Status reads or a processor reset. A read of the Thermal Status Word always includes a log bit clear mask that allows the host to clear any or all log bits that it is interested in tracking.

A bit set to 0b0 in the log bit clear mask will result in clearing the associated log bit. If a mask bit is set to 0b0 and that bit is not a legal mask, a failing completion code will be returned. A bit set to 0b1 is ignored and results in no change to any sticky log bits. For example, to clear the TCC Activation Log bit and retain all other log bits, the Thermal Status Read should send a mask of 0xFFFFFFFD.

Figure 7-23. Thermal Status Word



7.3.2.6.4 Counter Snapshot / Read / Clear

A reference time and 'Thermally Constrained' time are managed in the processor. These two counters are managed via the Mailbox. These counters are valuable for detecting thermal runaway conditions where the TCC activation duty cycle reaches excessive levels.

The counters may be simultaneously snapshot, simultaneously cleared, or independently read. Each counter is 32-bits wide.

Table 7-26. Counter Definition

Counter Name	Counter Number	Definition
Total Time	0x00	Counts the total time the processor has been executing with a resolution of approximately 1ms. This counter wraps at 32 bits.
Thermally Constrained Time	0x01	Counts the total time the processor has been operating at a lowered performance due to TCC activation. This timer includes the time required to ramp back up to the original P-state target after TCC activation expires. This timer does not include TCC activation time as a result of an external assertion of PROCHOT#.

7.3.2.6.5 Icc-TDC Read

Icc-TDC is the processor Thermal Design Current specification. This data may be used to confirm matching Icc profiles of processors in DP configurations. It may also be used during the processor boot sequence to verify processor compatibility with baseboard Icc delivery capabilities.

This command returns Icc-TDC in units of 1 Amp.

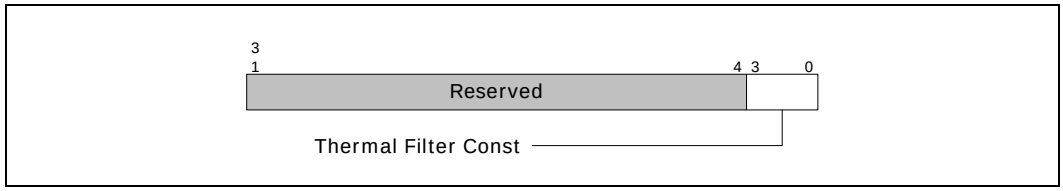
7.3.2.6.6 TCONTROL Read

TCONTROL is used for fan speed control management. The TCONTROL limit may be read over PECI using this Mailbox function. Unlike the in-band MSR interface, this TCONTROL value is already adjusted to be in the native PECI temperature format of a 2-byte, 2's complement number.

7.3.2.6.7 Thermal Data Config Read / Write

The Thermal Data Configuration register allows the PECI host to control the window over which thermal data is filtered. The default window is 256 ms. The host may configure this window by writing a Thermal Filtering Constant as a power of two. E.g., sending a value of 9 results in a filtering window of 2^9 or 512 ms.

Figure 7-24. Thermal Data Configuration Register



7.3.2.6.8 Machine Check Read

PECI offers read access to all processor machine check banks. Bank numbers 2, 3, 4 and 5 are all associated with cores and therefore the appropriate core select must be sent along with the Machine Check Read request. For all other Machine Check banks, the Core Select must be set to 0x0.

It is possible that a fatal error may prevent access to other machine check banks. Host controllers may read Power Control Unit errors directly by issuing a PCIConfigRd() command of address 0x000000B0.

Figure 7-25. Machine Check Read MbxSend() Data Format

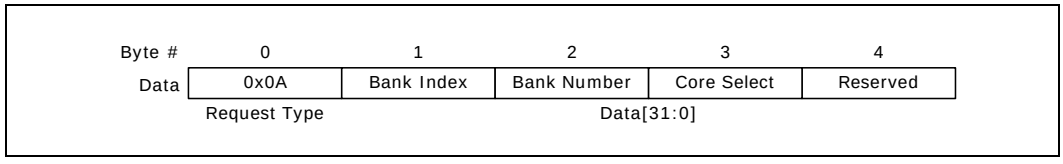


Table 7-27. Machine Check Bank Definitions (Sheet 1 of 3)

Bank Number	Bank Index	Meaning
0	0	MC0_CTL[31:0]
0	1	MC0_CTL[63:32]
0	2	MC0_STATUS[31:0]
0	3	MC0_STATUS[63:32]

Table 7-27. Machine Check Bank Definitions (Sheet 2 of 3)

Bank Number	Bank Index	Meaning
0	4	MC0_ADDR[31:0]
0	5	MC0_ADDR[63:32]
0	6	MC0_MISC[31:0]
0	7	MC0_MISC[63:32]
1	0	MC1_CTL[31:0]
1	1	MC1_CTL[63:32]
1	2	MC1_STATUS[31:0]
1	3	MC1_STATUS[63:32]
1	4	MC1_ADDR[31:0]
1	5	MC1_ADDR[63:32]
1	6	MC1_MISC[31:0]
1	7	MC1_MISC[63:32]
2	0	MC2_CTL[31:0]
2	1	MC2_CTL[63:32]
2	2	MC2_STATUS[31:0]
2	3	MC2_STATUS[63:32]
2	4	MC2_ADDR[31:0]
2	5	MC2_ADDR[63:32]
2	6	MC2_MISC[31:0]
2	7	MC2_MISC[63:32]
3	0	MC3_CTL[31:0]
3	1	MC3_CTL[63:32]
3	2	MC3_STATUS[31:0]
3	3	MC3_STATUS[63:32]
3	4	MC3_ADDR[31:0]
3	5	MC3_ADDR[63:32]
3	6	MC3_MISC[31:0]
3	7	MC3_MISC[63:32]
4	0	MC4_CTL[31:0]
4	1	MC4_CTL[63:32]
4	2	MC4_STATUS[31:0]
4	3	MC4_STATUS[63:32]
4	4	MC4_ADDR[31:0]
4	5	MC4_ADDR[63:32]
4	6	MC4_MISC[31:0]
4	7	MC4_MISC[63:32]
5	0	MC5_CTL[31:0]
5	1	MC5_CTL[63:32]
5	2	MC5_STATUS[31:0]
5	3	MC5_STATUS[63:32]
5	4	MC5_ADDR[31:0]
5	5	MC5_ADDR[63:32]

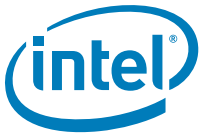


Table 7-27. Machine Check Bank Definitions (Sheet 2 of 3)

Bank Number	Bank Index	Meaning
0	4	MC0_ADDR[31:0]
0	5	MC0_ADDR[63:32]
0	6	MC0_MISC[31:0]
0	7	MC0_MISC[63:32]
1	0	MC1_CTL[31:0]
1	1	MC1_CTL[63:32]
1	2	MC1_STATUS[31:0]
1	3	MC1_STATUS[63:32]
1	4	MC1_ADDR[31:0]
1	5	MC1_ADDR[63:32]
1	6	MC1_MISC[31:0]
1	7	MC1_MISC[63:32]
2	0	MC2_CTL[31:0]
2	1	MC2_CTL[63:32]
2	2	MC2_STATUS[31:0]
2	3	MC2_STATUS[63:32]
2	4	MC2_ADDR[31:0]
2	5	MC2_ADDR[63:32]
2	6	MC2_MISC[31:0]
2	7	MC2_MISC[63:32]
3	0	MC3_CTL[31:0]
3	1	MC3_CTL[63:32]
3	2	MC3_STATUS[31:0]
3	3	MC3_STATUS[63:32]
3	4	MC3_ADDR[31:0]
3	5	MC3_ADDR[63:32]
3	6	MC3_MISC[31:0]
3	7	MC3_MISC[63:32]
4	0	MC4_CTL[31:0]
4	1	MC4_CTL[63:32]
4	2	MC4_STATUS[31:0]
4	3	MC4_STATUS[63:32]
4	4	MC4_ADDR[31:0]
4	5	MC4_ADDR[63:32]
4	6	MC4_MISC[31:0]
4	7	MC4_MISC[63:32]
5	0	MC5_CTL[31:0]
5	1	MC5_CTL[63:32]
5	2	MC5_STATUS[31:0]
5	3	MC5_STATUS[63:32]
5	4	MC5_ADDR[31:0]
5	5	MC5_ADDR[63:32]

Table 7-27. Machine Check Bank Definitions (Sheet 3 of 3)

Bank Number	Bank Index	Meaning
5	6	MC5_MISC[31:0]
5	7	MC3_MISC[63:32]
6	0	MC6_CTL[31:0]
6	1	MC6_CTL[63:32]
6	2	MC6_STATUS[31:0]
6	3	MC6_STATUS[63:32]
6	4	MC6_ADDR[31:0]
6	5	MC6_ADDR[63:32]
6	6	MC6_MISC[31:0]
6	7	MC6_MISC[63:32]
8	0	MC8_CTL[31:0]
8	1	MC8_CTL[63:32]
8	2	MC8_STATUS[31:0]
8	3	MC8_STATUS[63:32]
8	4	MC8_ADDR[31:0]
8	5	MC8_ADDR[63:32]
8	6	MC8_MISC[31:0]
8	7	MC8_MISC[63:32]

7.3.2.6.9 T-state Throttling Control Read / Write

PECI offers the ability to enable and configure ACPI T-state (core clock modulation) throttling. ACPI T-state throttling forces all CPU cores into duty cycle clock modulation where the core toggles between C0 (clocks on) and C1 (clocks off) states at the specified duty cycle. This throttling reduces CPU performance to the duty cycle specified and, more importantly, results in processor power reduction.

The processor supports software initiated T-state throttling and automatic T-state throttling as part of the internal Thermal Monitor response mechanism (upon TCC activation). The PECI T-state throttling control register read/write capability is managed only in the PECI domain. In-band software may not manipulate or read the PECI T-state control setting. In the event that multiple agents are requesting T-state throttling simultaneously, the CPU always gives priority to the lowest power setting, or the numerically lowest duty cycle.

The only supported duty cycle is 12.5% (12.5% clocks on, 87.5% clocks off). It is expected that T-state throttling will be engaged only under emergency thermal or power conditions. Future products may support more duty cycles, as defined in the following table:

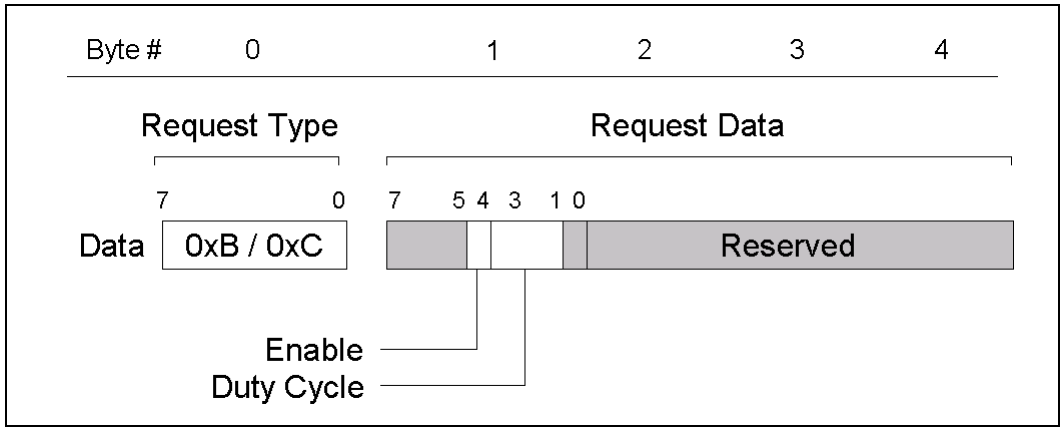
Table 7-28. ACPI T-state Duty Cycle Definition

Duty Cycle Code	Definition
0x0	Undefined
0x1	**12.5% clocks on / 87.5% clocks off**
0x2	25% clocks on / 75% clocks off
0x3	37.5% clocks on / 62.5% clocks off

Duty Cycle Code	Definition
0x4	50% clocks on / 50% clocks off
0x5	62.5% clocks on / 37.5% clocks off
0x6	75% clocks on / 25% clocks off
0x7	87.5% clocks on / 12.5% clocks off

The T-state control word is defined as follows:

Figure 7-26. ACPI T-State Throttling Control Read / Write Definition



7.3.2.6.10 Energy Accumulator Read

Intel Xeon processor 5600 series energy consumption may be monitored with regular reads of the free running Energy Accumulator. The Energy Accumulator reports processor energy consumed on the VCC, VTT, VCCPLL and VDD power rails in Joules in an unsigned, 32-bit fixed point binary format. The least-significant 16 bits report the fractional data and the most significant 16 bits report the integer data. Because the Energy Accumulator is constantly incrementing, the data is only relevant as a delta between two subsequent reads.

Overflow in the accumulator is infrequent, but it will occur constantly during normal execution. Therefore, the PECI host controller or firmware must be designed such that it can guarantee a polling rate sufficient to prevent aliasing. Recommended polling rates are between 1Hz and 10Hz. As an example, a processor steadily consuming 130 W of power will overflow the accumulator once every 8.4 minutes.

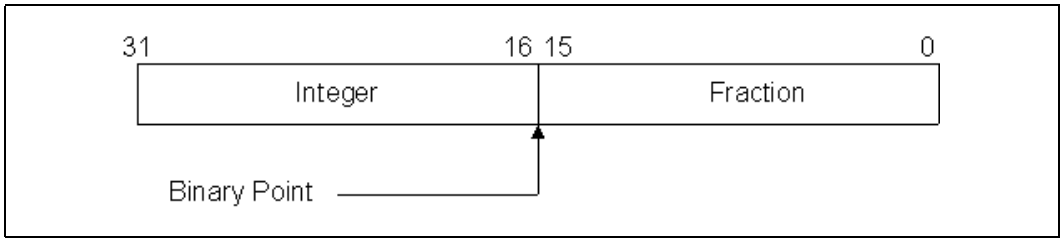
The free running nature of the PECI Energy Accumulator register allows for irregular timing on reads. It is expected that the PECI host controller or firmware will manage its own time stamps.

Accuracy of the Energy Accumulator may be processor or platform specific, and is a function of the Voltage Regulator IMON solution.

On processor power-up, the Energy Accumulator Register is reset to 0x0. On all subsequent processor resets where power is maintained to processor, the accumulator continues to count uninterrupted.

The Energy Accumulator register is defined as follows:

Figure 7-27. Energy Accumulator Register Definition



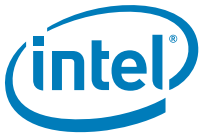
Example 7-1.Sample Energy Accumulator Read and Power Calculation.

Time: 127 ms

```
TransID = MbxSend(0x0F, 0x0)
EnergyAccumulated[0] = MbxGet(TransID)
    EnergyAccumulated[0] = 0xfff737a3
```

Time: 228 ms

```
TransID = MbxSend(0x0F, 0x0)
EnergyAccumulated[1] = MbxGet(TransID)
    EnergyAccumulated[0] = 0x00176dc
if (EnergyAccumulated[1] < EnergyAccumulated[0]) {
    Joules = EnergyAccumulated[1] + 0xffffffff - EnergyAccumulated[0]
    Joules = 0x00176dc + 0xffffffff - 0xfff737a3 = 10.2469 J
    Watts = 10.2469 / (.228 - .127) = 101.455 W
}
else {
    Joules = EnergyAccumulated[1] - EnergyAccumulated[0]
}
```



This capability may not be available on all products. To enumerate availability, users may issue an Energy Accumulator Read command. Products that return a passing completion code support the command.

7.3.2.7 MbxSend()

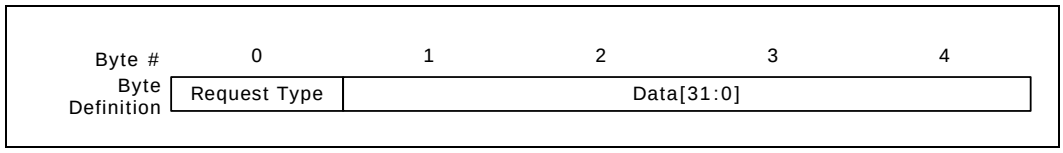
The MbxSend() command is utilized for sending requests to the generic Mailbox interface. Those requests are in turn serviced by the processor with some nominal latency and the result is deposited in the mailbox for reading. MbxGet() is used to retrieve the response and details are documented in Section 7.3.2.8.

The details of processor mailbox capabilities are described in Section 7.3.2.6.1, and many of the fundamental concepts of Mailbox ownership, release, and management are discussed in Section 7.3.2.9.

7.3.2.7.1 Write Data

Regardless of the function of the mailbox command, a request type modifier and 4-byte data payload must be sent. For Mailbox commands where the 4-byte data field is not applicable (e.g., the command is a read), the data written should be all zeroes.

Figure 7-28. MbxSend() Command Data Format



Because a particular MbxSend() command may specify an update to potentially critical registers inside the processor, it includes an Assured Write FCS (AW FCS) byte as part of the write data payload. In the event that the AW FCS mismatches with the client-calculated FCS, the client will abort the write and will always respond with a bad Write FCS.

7.3.2.7.2 Command Format

The MbxSend() format is as follows:

Write Length: 7

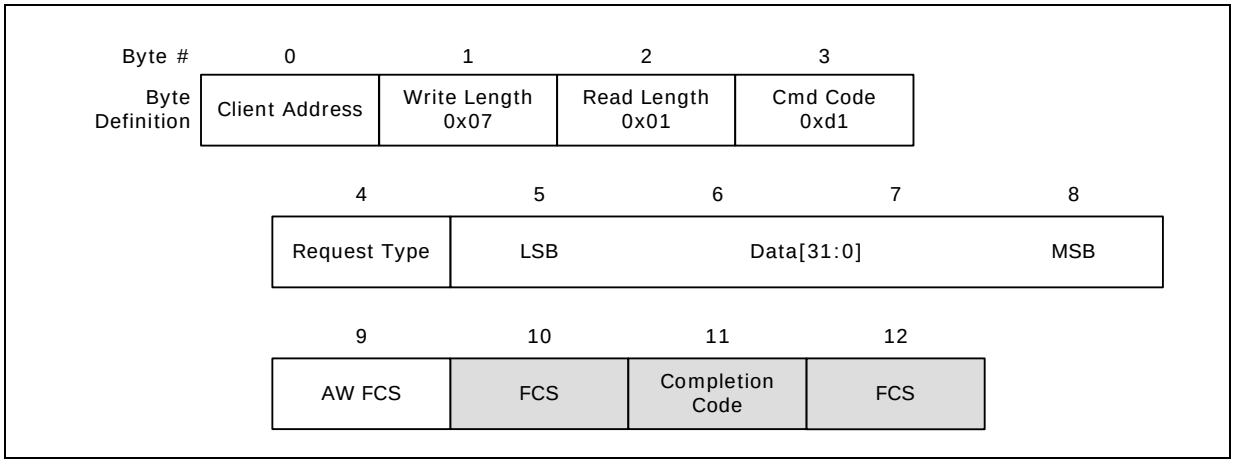
Read Length: 1

Command: 0xd1

Multi-Domain Support: Yes (see Table 7-32)

Description: Deposits the Request Type and associated 4-byte data in the Mailbox interface and returns a completion code byte with the details of the execution results. Refer to Section 7.3.4.2 for completion code definitions.

Figure 7-29. MbxSend()



Note that the 4-byte data defined above is sent in standard PECI ordering with LSB first and MSB last.

Table 7-29. MbxSend() Response Definition

Response	Meaning
Bad FCS	Electrical error
0x4X	Semaphore is granted with a Transaction ID of 'X'
0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET condition or processor S1 state. Retry is appropriate outside of the RESET or S1 states.
0x86	Mailbox interface is unavailable or busy

If MbxSend() response returns a bad FCS in the data, the completion code can't be trusted and the semaphore may or may not be taken. In order to clean out the interface, an MbxGet() must be issued and the response data should be discarded.

7.3.2.8 MbxGet()

The MbxGet() command is utilized for retrieving response data from the generic Mailbox interface as well as for unlocking the acquired mailbox. Please refer to Section 7.3.2.7 for details regarding the MbxSend() command. Many of the fundamental concepts of Mailbox ownership, release, and management are discussed in Section 7.3.2.9.

7.3.2.8.1 Write Data

The MbxGet() command is designed to retrieve response data from a previously deposited request. In order to guarantee alignment between the temporally separated request (MbxSend) and response (MbxGet) commands, the originally granted Transaction ID (sent as part of the passing MbxSend() completion code) must be issued as part of the MbxGet() request.

Any mailbox request made with an illegal or unlocked Transaction ID will get a failed completion code response. If the Transaction ID matches an outstanding transaction ID associated with a locked mailbox, the command will complete successfully and the response data will be returned to the originator.

Unlike MbxSend(), no Assured Write protocol is necessary for this command because this is a read-only function.

7.3.2.8.2 Command Format

The MbxGet() format is as follows:

Write Length: 2

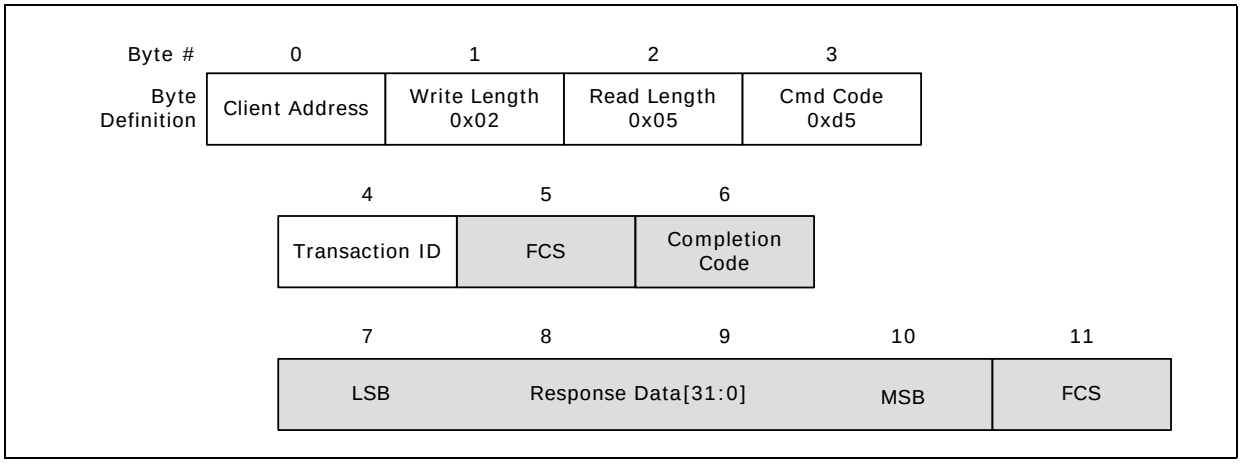
Read Length: 5

Command: 0xd5

Multi-Domain Support: Yes (see Table 7-32)

Description: Retrieves response data from mailbox and unlocks / releases that mailbox resource.

Figure 7-30. MbxGet()



Note that the 4-byte data response defined above is sent in standard PECI ordering with LSB first and MSB last.

Table 7-30. MbxGet() Response Definition (Sheet 1 of 2)

Response	Meaning
Aborted Write FCS	Response data is not ready. Command retry is appropriate.
0x40	Command passed, data is valid
0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET condition or processor S1 state. Retry is appropriate outside of the RESET or S1 states.
0x81	Thermal configuration data was malformed or exceeded limits.
0x82	Thermal status mask is illegal
0x83	Invalid counter select
0x84	Invalid Machine Check Bank or Index
0x85	Failure due to lack of Mailbox lock or invalid Transaction ID
0x86	Mailbox interface is unavailable or busy

Table 7-30. MbxGet() Response Definition (Sheet 2 of 2)

Response	Meaning
0x88	Machine Check Banks is currently unavailable (selected core is asleep or unavailable)
0x89	Invalid Core Select for Machine Check Bank Read
0xFF	Unknown/Invalid Mailbox Request

7.3.2.9 Mailbox Usage Definition

7.3.2.9.1 Acquiring the Mailbox

The MbxSend() command is used to acquire control of the PECI mailbox and issue information regarding the specific request. The completion code response indicates whether or not the originator has acquired a lock on the mailbox, and that completion code always specifies the Transaction ID associated with that lock (see Section 7.3.2.9.2).

Once a mailbox has been acquired by an originating agent, future requests to acquire that mailbox will be denied with an 'interface busy' completion code response.

The lock on a mailbox is not achieved until the last bit of the MbxSend() Read FCS is transferred (in other words, it is not committed until the command completes). If the host aborts the command at any time prior to that bit transmission, the mailbox lock will be lost and it will remain available for any other agent to take control.

7.3.2.9.2 Transaction ID

For all MbxSend() commands that complete successfully, the passing completion code (0x4X) includes a 4-bit Transaction ID ('X'). That ID is the key to the mailbox and must be sent when retrieving response data and releasing the lock by using the MbxGet() command.

The Transaction ID is generated internally by the processor and has no relationship to the originator of the request. On Intel® Xeon® processor 5600 series, only a single outstanding Transaction ID is supported. Therefore, it is recommended that all devices requesting actions or data from the Mailbox complete their requests and release their semaphore in a timely manner.

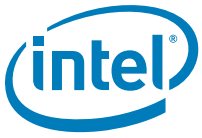
In order to accommodate future designs, software or hardware utilizing the PECI mailbox must be capable of supporting Transaction IDs between 0 and 15.

7.3.2.9.3 Releasing the Mailbox

The mailbox associated with a particular Transaction ID is only unlocked / released upon successful transmission of the last bit of the Read FCS. If the originator aborts the transaction prior to transmission of this bit (presumably due to an FCS failure), the semaphore is maintained and the MbxGet() command may be retried.

7.3.2.9.4 Mailbox Timeouts

The mailbox is a shared resource that can result in artificial bandwidth conflicts among multiple querying processes that are sharing the same originator interface. The interface response time is quick, and with rare exception, back to back MbxSend() and MbxGet() commands should result in successful execution of the request and release of the mailbox. In order to guarantee timely retrieval of response data and mailbox release, the mailbox semaphore has a timeout policy. If the PECI bus has a cumulative '0 time of 1ms since the semaphore was acquired, the semaphore is automatically



cleared. In the event that this timeout occurs, the originating agent will receive a failed completion code upon issuing a MbxGet() command, or even worse, it may receive corrupt data if this MbxGet() command so happens to be interleaved with an MbxSend() from another process. Please refer to Table 7-30 for more information regarding failed completion codes from MbxGet() commands.

Timeouts are undesirable, and the best way to avoid them and guarantee valid data is for the originating agent to always issue MbxGet() commands immediately following MbxSend() commands.

If the timeout policy is too restrictive, it can be disabled. BIOS may write MSR_MISC_POWER_MGMT (0x1AA), bit 11 to 0b1 in order to force a disable of this automatic timeout.

7.3.2.9.5 Response Latency

The PECI mailbox interface is designed to have response data available within plenty of margin to allow for back-to-back MbxSend() and MbxGet() requests. However, under rare circumstances that are out of the scope of this specification, it is possible that the response data is not available when the MbxGet() command is issued. Under these circumstances, the MbxGet() command will respond with an Abort FCS and the originator should re-issue the MbxGet() request.

7.3.3 Multi-Domain Commands

The Intel Xeon processor 5600 series does not support multiple domains, but it is possible that future products will, and the following tables are included as a reference for domain-specific definitions.

Table 7-31. Domain ID Definition

Domain ID	Domain Number
0b01	**0**
0b10	1

Table 7-32. Multi-Domain Command Code Reference

Command Name	Domain 0 Code	Domain 1 Code
GetTemp()	**0x01**	0x02
PCIConfigRd()	**0xC1**	0xC2
PCIConfigWr()	**0xC5**	0xC6
MbxSend()	**0xD1**	0xD2
MbxGet()	**0xD5**	0xD6

7.3.4 Client Responses

7.3.4.1 Abort FCS

The Client responds with an Abort FCS under the following conditions:

- The decoded command is not understood or not supported on this processor (this includes good command codes with bad Read Length or Write Length bytes).
- Data is not ready.

- Assured Write FCS (AW FCS) failure. Note that under most circumstances, an Assured Write failure will appear as a bad FCS. However, when an originator issues a poorly formatted command with a miscalculated AW FCS, the client will intentionally abort the FCS in order to guarantee originator notification.

7.3.4.2 Completion Codes

Some PECI commands respond with a completion code byte. These codes are designed to communicate the pass/fail status of the command and also provide more detailed information regarding the class of pass or fail. For all commands listed in Section 7.3.2 that support completion codes, each command's completion codes is listed in its respective section. What follows are some generalizations regarding completion codes.

An originator that is decoding these commands can apply a simple mask to determine pass or fail. Bit 7 is always set on a failed command, and is cleared on a passing command.

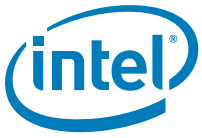
Table 7-33. Completion Code Pass/Fail Mask

0xxx xxxxb	Command passed
1xxx xxxxb	Command failed

Table 7-34. Device Specific Completion Code (CC) Definition

Completion Code	Description
0x00..0x3F	Device specific pass code
0x40	Command Passed
0x4X	Command passed with a transaction ID of 'X' (0x40 | Transaction_ID[3:0])
0x50..0x7F	Device specific pass code
0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET condition or processor S1 state. Retry is appropriate outside of the RESET or S1 states.
0x81	Thermal configuration data was malformed or exceeded limits.
0x82	Thermal status mask is illegal
0x83	Invalid counter select
0x84	Invalid Machine Check Bank or Index
0x85	Failure due to lack of Mailbox lock or invalid Transaction ID
0x86	Mailbox interface is unavailable or busy
0x88	Machine Check Banks is currently unavailable (selected core is asleep or unavailable)
0x89	Invalid Core Select for Machine Check Bank Read
0xFF	Unknown/Invalid Request

Note: The codes explicitly defined in this table may be useful in PECI originator response algorithms. All reserved or undefined codes may be generated by a PECI client device, and the originating agent must be capable of tolerating any code. The Pass/Fail mask defined in Table 7-33 applies to all codes and general response policies may be based on that limited information.



7.3.5 Originator Responses

The simplest policy that an originator may employ in response to receipt of a failing completion code is to retry the request. However, certain completion codes or FCS responses are indicative of an error in command encoding and a retry will not result in a different response from the client. Furthermore, the message originator must have a response policy in the event of successive failure responses.

Please refer to the definition of each command in Section 7.3.2 for a specific definition of possible command codes or FCS responses for a given command. The following response policy definition is generic, and more advanced response policies may be employed at the discretion of the originator developer.

Table 7-35. Originator Response Guidelines

Response	After 1 Attempt	After 3 Attempts...
Bad FCS	Retry	Fail with PECI client device error
Abort FCS	Retry	Fail with PECI client device error. May be due to illegal command codes.
Fail	Retry	Either the PECI client doesn't support the current command code, or it has failed in its attempts to construct a response.
None (all 0's)	Force bus idle (1ms low), retry	Fail with PECI client device error. Client may be dead or otherwise non-responsive (in RESET or S1, for example).
Pass	Pass	NA
Good FCS	Pass	NA

7.3.6 Temperature Data

7.3.6.1 Format

The temperature is formatted in a 16-bit, 2's complement value representing a number of 1/64 degrees centigrade. This format allows temperatures in a range of ±512°C to be reported to approximately a 0.016°C resolution.

Figure 7-31. Temperature Sensor Data Format

MSB Upper nibble					MSB Lower nibble					LSB Upper nibble					LSB Lower nibble			
S	x	x	x		x	x	x	x		x	x	x	x		x	x	x	x
Sign	Integer Value (0-511)											Fractional Value (~0.016)						

7.3.6.2 Interpretation

The resolution of the processor's Digital Thermal Sensor (DTS) is approximately 1°C, which can be confirmed by a RDMSR from IA32_THERM_STATUS MSR (0x19C) where it is architecturally defined. PECI temperatures are sent through a configurable low-pass filter prior to delivery in the GetTemp() response data. The output of this filter produces temperatures at the full 1/64°C resolution even though the DTS itself is not this accurate.

Temperature readings from the processor are always negative, and imply an offset from the reference TCC activation temperature. As an example, assume that the TCC activation temperature reference is 100°C. A PECI thermal reading of -10°C indicates that the processor is running at 10°C below the TCC activation temperature, or 90°C.

PECI temperature readings are not reliable at temperatures above TCC activation (since the processor is operating out of spec at this temperature). Therefore, the readings are never positive.

7.3.6.3 Temperature Filtering

The processor digital thermal sensor (DTS) provides an improved capability to monitor device hot spots, which inherently leads to more varying temperature readings over short time intervals. Coupled with the fact that typical fan speed controllers may only read temperatures at 4 Hz, it is necessary for the thermal readings to reflect thermal trends and not instantaneous readings. Therefore, PECI supports a configurable low-pass temperature filtering function. By default, this filter results in a thermal reading that is a moving average of 256 samples taken at approximately 1msec intervals. This filter's depth, or smoothing factor, may be configured to between 1 sample and 1024 samples, in powers of 2. See the equation below for reference where the configurable variable is 'X'.

$$T_N = T_{N-1} + 1/2^X * (T_{SAMPLE} - T_{N-1})$$

Please refer to Section 7.3.2.6 for the definition of the thermal configuration command.

7.3.6.4 Reserved Values

Several values well out of the operational range are reserved to signal temperature sensor errors. These are summarized in the table below:

Table 7-36. Error Codes and Descriptions

Error Code	Description
0x8000	General Sensor Error (GSE)

7.3.7 Client Management

7.3.7.1 Power-Up Sequencing

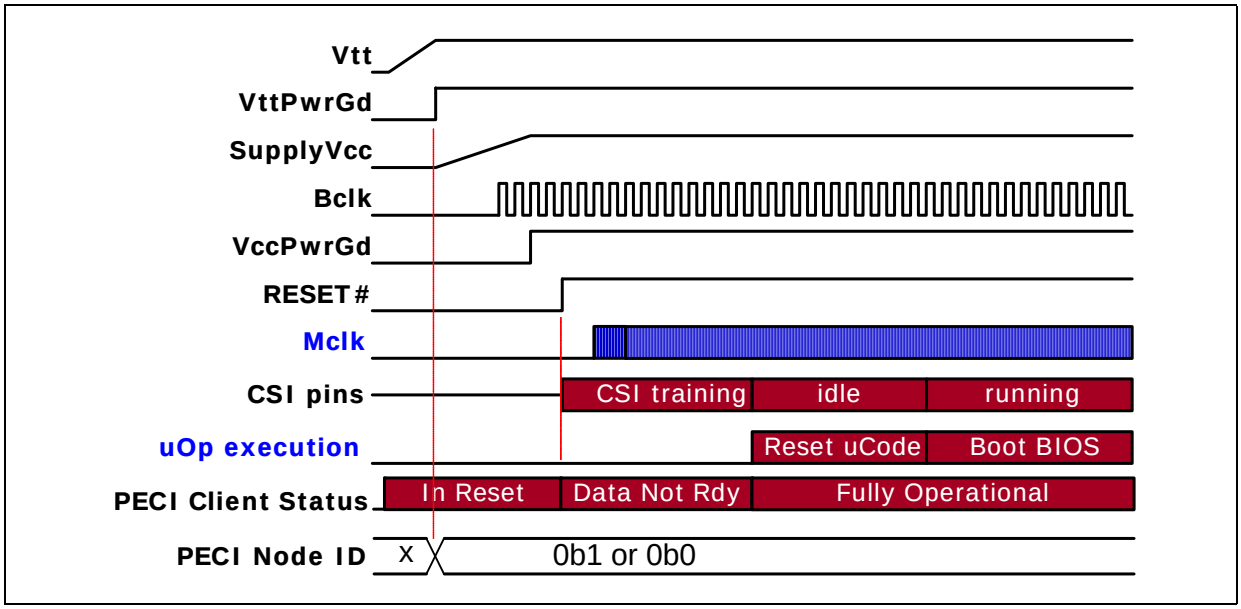
The PECI client is fully reset during processor RESET# assertion. This means that any transactions on the bus will be completely ignored, and the host will read the response from the client as all zeroes. After processor RESET# deassertion, the Intel Xeon processor 5600 series PECI client is operational enough to participate in timing negotiations and respond with reasonable data. However, the client data is not guaranteed to be fully populated until approximately 500 µs after processor RESET# is deasserted. Until that time, the client responses to each command are as follows:

Table 7-37. PECI Client Response During Power-Up (During 'Data Not Ready')

Command	Response
Ping()	Fully functional
GetDIB()	Fully functional
GetTemp()	Client responds with a 'hot' reading, or 0x0000
PCIConfigRd()	Fully functional
PCIConfigWr()	Fully functional
MbxSend()	Fully functional
MbxGet()	Client responds with Abort FCS (if MbxSend() has been previously issued)

In the event that the processor is tri-stated using power-on-configuration controls, the PECI client will also be tri-stated.

Figure 7-32. PECI Power-Up Timeline



7.3.7.2 Device Discovery

The PECI client is available on all processors, and positive identification of the PECI revision number can be achieved by issuing the GetDIB() command. Please refer to Section 7.3.2.2 for details on GetDIB response formatting.

7.3.7.3 Client Addressing

The PECI client assumes a default address of 0x30. If nothing special is done to the processor, all PECI clients will boot with this address. For DP enabled parts, a special PECI_ID# pin is available to strap each PECI socket to a different node ID. The package pin strap is evaluated at the assertion of VCCPWRGOOD (as depicted in Figure 7-32). Since PECI_ID# is active low, tying the pin to ground results in a client address of 0x31, and tying it to V_{TT} results in a client address of 0x30.

The client address may not be changed after VCCPWRGOOD assertion, until the next power cycle on the processor. Removal of a processor from its socket or tri-stating a processor in a DP configuration will have no impact to the remaining non-tri-stated PECI client address.

7.3.7.4 C-States

The Intel Xeon processor 5600 series are fully functional under all core and package C-states. Support for package C-states is a function of processor SKU and platform capabilities. All package C-states (C1E, C3, C6) are documented here for completeness, but actual processor support for these C-states may vary.

Because the processor takes aggressive power savings actions under the deepest C-states, PECI requests may have an impact to platform power. The impact is documented below:

- Ping(), GetDIB(), GetTemp() and MbxGet() have no impact on processor power under C-states. All other commands (MbxSend(), PCIConfigRd() and PCIConfigWr()) result in the same behavior, as follows:
- MbxSend(), PCIConfigRd() and PCIConfigWr() usage under package C-states may result in increased power consumption because the processor must temporarily return to a C0 state in order to execute the request. The exact power impact of a pop-up to C0 varies by product SKU, the C-state from which the pop-up is initiated, and the negotiated T_{BIT}.

7.3.7.5 S-States

The PECI client is always guaranteed to be operational under S0 and S1 sleep states. Under S3 and deeper sleep states, the PECI client response is undefined and therefore unreliable.

7.3.7.6 Processor Reset

Intel Xeon processor 5600 series acting as PECI clients are fully reset on all RESET# assertions. Upon deassertion of RESET#, where power is maintained to the processor (otherwise known as a 'warm reset'), the following are true:

- The PECI client assumes a bus Idle state.
- The Thermal Filtering Constant is retained.
- PECI Node ID is retained.
- GetTemp() reading resets to 0x0000.
- Any transaction in progress is aborted by the client (as measured by the client no longer participating in the response).
- The processor client is otherwise reset to a default configuration.

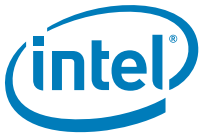
7.4 Storage Conditions Specifications

Environmental storage condition limits define the temperature and relative humidity limits to which the device is exposed to while being stored. The specified storage conditions are for component level prior to board attached (see following notes on post board attach limits).

Table 7-38 specifies absolute maximum and minimum storage temperature limits which represent the maximum and minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. At conditions outside sustained limits, but within absolution maximum and minimum ratings, quality & reliability may be affected.

Table 7-38. Storage Condition Ratings

Symbol	Parameter	Min	Max	Notes
$T_{abs\ storage}$	The minimum/maximum device storage temperature beyond which damage (latent or otherwise) may occur when subjected to for any length of time.	-55 °C	125 °C	1,2,3,4,5
$T_{sustained\ storage}$	The minimum/maximum device storage temperature for a sustained period of time.	-5 °C	40 °C	1,2,3,4,5
$RH_{sustained\ storage}$	The maximum device storage relative humidity for a sustained period of time.		60% @ 24 °C	1,2,3,4,5
$TIME_{sustained\ storage}$		0 months	6 months	1,2,3,4,5



Notes:
1. Storage conditions are applicable to storage environments only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
2. These ratings apply to the Intel component and do not include the tray or packaging.
3. Failure to adhere to this specification can affect the long-term reliability of the processor.
4. Non operating storage limits post board attache: Storage conditions limits for the component once attached to the application board are not specified.

Device storage temperature qualification methods follow JESD22-A119 (low temperature) and JESD22-A103 (high temperature) standards.

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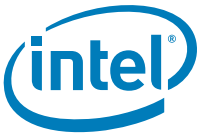


8 Features

8.1 Power-On Configuration (POC)

Several configuration options can be configured by hardware. Power-On configuration (POC) functionality is either MUx'ed onto VID signals (see Section 2.1.7.3.1) or sampled on the active-to-inactive transition of RESET#. For specifics on these options, please refer to Table 8-1.

Please note that requests to execute Built-In Self Test (BIST) are not selected by hardware, but rather passed across the Intel® QuickPath Interconnect link during initialization.

Table 8-1. Power-On Configuration Signal Options

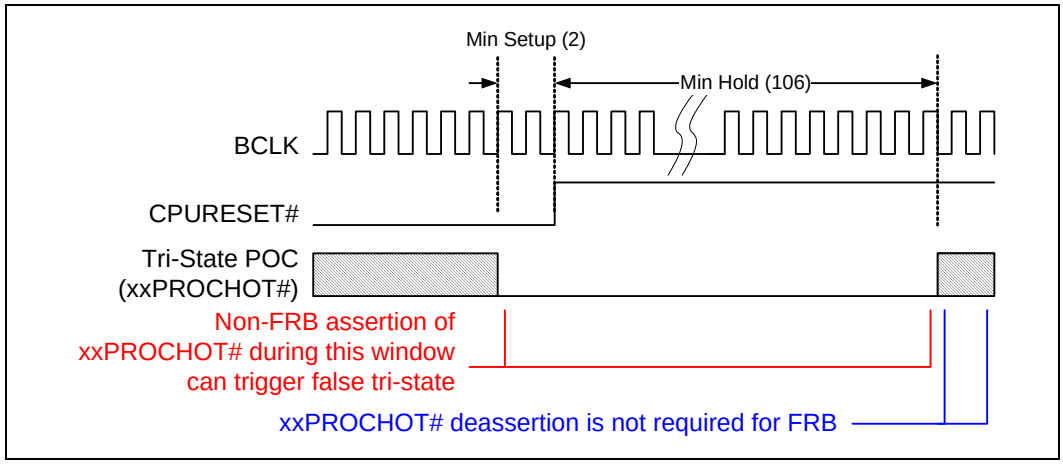
Configuration Option	Signal	Figure
Output tri-state	PROCHOT#[1]	8-1
PECI_ID#	PECI_ID#[2]	
Market Segment Identification (MSID)	VID[2:0] / MSID[2:0][2]	8-2
Current Sensor Configuration (CSC)	VID[5:3] / CSC[2:0][2]	

Notes:

1. Asserting the signal during RESET# de-assertion will select the corresponding option. Once selected, this option cannot be changed except via another reset. The processor does not distinguish between a "warm" reset and a "power-on" reset. Output tri-state via the PROCHOT# power-on configuration option is referred to as Fault Resilient Boot (FRB).
2. Latched when VTTPWRGOOD is asserted and all internal power good conditions are met.

Assertion of the PROCHOT# signal through RESET# de-assertion (also referred to as Fault Resilient Boot (FRB)) will tri-state processor outputs. Figure 8-1 outlines timing requirements when utilizing PROCHOT# as a power-on configuration option. In the event an FRB is desired, PROCHOT# and RESET# should be asserted simultaneously. Furthermore, once asserted, PROCHOT# should remain low long enough to meet the TH: Power-On Configuration Hold Time (PROCHOT#) as outlined in Table 2-26. Failure to do so may result in false tri-state.

Figure 8-1. PROCHOT# POC Timing Requirements



Note:

1. FRB = Fault-Resilient Boot

Power-On Configuration (POC) logic levels are MUX'ed onto the VID[7:0] signals with 1-5 kΩ pull-up and pull-down resistors located on the baseboard. These include:

- VID[2:0] / MSID[2:0] = Market Segment ID
- VID[5:3] / CSC [2:0] = Current Sense Configuration
- VID[6] = Reserved
- VID[7] = VR11.1 Select

Pull-up and pull-down resistors on the baseboard eliminate the need for timing specifications. After OUTEN signal is asserted, the VID[7:0] CMOS drivers (typically 50 Ω up/down impedance) over-ride the POC pull-up/down resistors located on the baseboard and drive the necessary VID pattern. Please refer to Table 2-3, "Power-On Configuration (POC[7:0]) Decode" for further details.

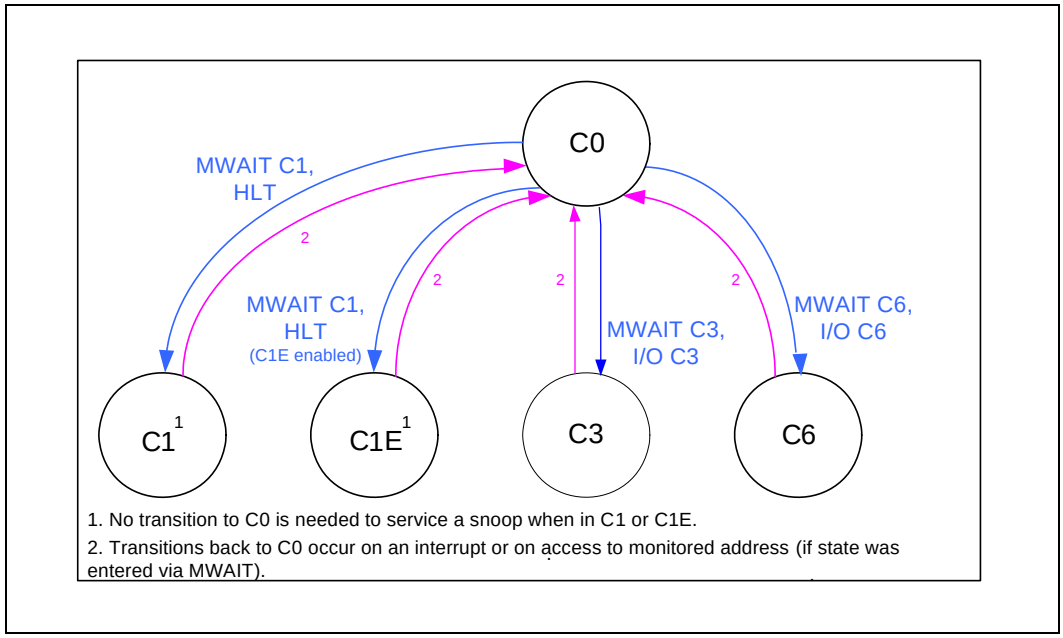
8.2 Clock Control and Low Power States

The processor supports low power states at the individual thread, core, and package level for optimal power management. The processor implements software interfaces for requesting low power states: MWAIT instruction extensions with sub-state hints, the HLT instruction (for C1 and C1E) and P_LVLx reads to the ACPI P_BLK register block mapped in the processor's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor and do not directly result in I/O reads to the system. The P_LVLx I/O Monitor address does not need to be set up before using the P_LVLx I/O read interface.

Note: Software may make C-state requests by using a legacy method involving I/O reads from the ACPI-defined processor clock control registers, referred to as P_LVLx. This feature is designed to provide legacy support for operating systems that initiate C-state transitions via access to pre-defined ICH registers. The base P_LVLx register is P_LVL2, corresponding to a C3 request. P_LVL3 is C6, and all P_LVL4+ are demoted to a C6.

P_LVLx is limited to a subset of C-states (For example, P_LVL8 is not supported and will not cause an I/O redirection to a C8 request. Instead, it will fall through like a normal I/O instruction). The range of I/O addresses that may be converted into C-state requests is also defined in the PMG_IO_CAPTURE MSR, in the 'C-state Range' field. This field maybe written by BIOS to restrict the range of I/O addresses that are trapped and redirected to MWAIT instructions. Note that when I/O instructions are used, no MWAIT substates can be defined, as therefore the request defaults to have a sub-state or zero, but always assumes the 'Break on EFLAGS.IF==0' control that can be selected using ECX with an MWAIT instruction.

Figure 8-2. Power States



8.2.1 Thread and Core Power State Descriptions

Individual threads may request low power states as described below. Core power states are automatically resolved by the processor as shown in Table 8-2.

Table 8-2. Coordination of Thread Power States at the Core Level

Core State	Thread 1 State			
Thread 0 State	**C0**	**C1[1]**	**C3**	**C6**
C0	C0	C0	C0	C0
C1[1]	C0	C1[1]	C1[1]	C1[1]
C3	C0	C1[1]	C3	C3
C6	C0	C1[1]	C3	C6

Note:
1. If enabled, state will be C1E.

8.2.1.1 C0 State

This is the normal operating state in the processor.

8.2.1.2 C1/C1E State

C1/C1E is a low power state entered when all threads within a core execute a HLT or MWAIT(C1E) instruction. The processor thread will transition to the C0 state upon occurrence of an interrupt or an access to the monitored address if the state was entered via the MWAIT instruction. RESET# will cause the processor to initialize itself.

A System Management Interrupt (SMI) handler will return execution to either Normal state or the C1 state. See the *Intel® 64 and IA-32 Architecture Software Developer's Manuals, Volume III: System Programmer's Guide* for more information.

While in C1/C1E state, the processor will process bus snoops and snoops from the other threads.

To operate within specification, BIOS must enable the C1E feature for all installed processors.

8.2.1.3 C3 State

Individual threads of the processor can enter the C3 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C3) instruction. Before entering core C3, that core flushes the contents of its caches. Caches shared among cores are not impacted. Except for the caches, the processor core maintains all its architectural state while in the C3 state. All of the clocks in the processor core are stopped in the C3 state.

Because the core's caches are flushed, the processor keeps the core in the C3 state when the processor detects a snoop on the Intel QuickPath Interconnect Link or when another logical processor in the same package accesses cacheable memory. The processor core will transition to the C0 state upon occurrence of an interrupt. RESET# will cause the processor core to initialize itself.

8.2.1.4 C6 State

Individual threads of the processor can enter the C6 state by initiating a P_LVL3 read to the P_BLK or an MWAIT(C6) instruction. Before entering core C6, that core flushes the contents of its caches. Caches shared among cores are not impacted. The processor achieves additional power savings in the core C6 state.

8.2.2 Package Power State Descriptions

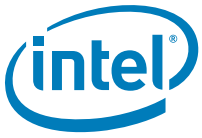
The package supports C0, C1/C1E, C3 and C6 power states. The package power state is automatically resolved by the processor depending on the core power states and permission from the rest of the system as described below.

8.2.2.1 Package C0 State

This is the normal operating state for the processor. The processor remains in the Normal state when at least one of its cores is in the C0 or C1 state or when another component in the system has not granted permission to the processor to go into a low power state. Individual components of the processor may be in low power states while the package in C0.

8.2.2.2 Package C1/C1E State

The package will enter the C1/C1E low power state when at least one core is in the C1/C1E state and the rest of the cores are in a C1/C1E or deeper power state. The processor will also enter the C1/C1E state when all cores are in a power state lower than C1/C1E but the package low power state is limited to C1/C1E via the PMG_CST_CONFIG_CONTROL MSR. In the C1E state, the processor will automatically transition to the lowest power operating point (lowest supported voltage and associated frequency). When entering the C1E state, the processor will first switch to the lowest bus ratio and then transition to the lower VID. No notification to the system occurs upon entry to C1/C1E.



8.2.2.3 Package C3 State

The package will enter the C3 low power state when all cores are in the C3 or lower power state and the processor has been granted permission by the other component(s) in the system to enter the C3 state. The package will also enter the C3 state when all cores are in an idle state lower than C3 but other component(s) in the system have only granted permission to enter C3.

If Intel® QuickPath Interconnect L1 has been granted, the processor will disable some clocks and PLLs and for processors with an integrated memory controller, the DRAM will be put into self-refresh.

8.2.2.4 Package C6 State

The package will enter the C6 low power state when all cores are in the C6 or lower power state and the processor has been granted permission by the other component(s) in the system to enter the C6 state. The package will also enter the C6 state when all cores are in an idle state lower than C6 but the other component(s) have only granted permission to enter C6.

If Intel® QuickPath Interconnect L1 has been granted, the processor will disable some clocks and PLLs. The shared cache will enter a deep sleep state. Additionally, for processors with an integrated memory controller, the DRAM will be put into self-refresh.

8.2.3 Intel Xeon Processor 5600 Series C-State Power Specifications

Table 8-3 lists C-state power specifications for various processor SKU's.

Table 8-3. Processor C-State Power Specifications

Package C-State[1]	Intel® Xeon® Processor 5600 Series				
	TDP=130 W	TDP=95W	TDP=80W[2]	TDP=60W	TDP=40W
C1E	37 W	32 W	37/40 W	25 W	22 W
C3	32 W	28 W	33/33 W	20 W	18 W
C6	12 W	10 W	12/14 W	8 W	8 W

Notes:
1. Specifications are at T_{CASE} = 50 °C with all cores in the specified C-state.
2. Standard/Basic SKUs.

8.3 Sleep States

The processor supports the ACPI sleep states S0, S1, S3, and S4/S5 as shown in Table 8-4. For information on ACPI S-states and related terminology, refer to the *Advanced Configuration and Power Interface Specification*. The S-state transitions are coordinated by the processor in response PM Request (PMReq) messages from the chipset. The processor itself will never request a particular S-state.

Table 8-4. Processor S-States

S-State	Power Reduction	Allowed Transitions
S0	Normal Code Execution	S1 (via PMReq)
S1	Cores in C1E like state, processor responds with CmpD(S1) message.	S0 (via reset or PMReq) S3, S4 (via PMReq)
S3	Memory put into self-refresh, processor responds with CmpD(S3) message.	S0 (via reset)
S4/S5	Processor responds with CmpD(S4/S5) message.	S0 (via reset)

Notes:
1. If the chipset requests an S-state transition which is not allowed, a machine check error will be generated by the processor.

8.4 Intel® Turbo Boost Technology

The processor supports ACPI P-states. A new feature, Intel® Turbo Boost Technology (Intel® TBT), allows the processor to opportunistically and automatically run faster than the marked frequency in ACPI P0 state if the part is operating below power, temperature and current limits. Max Turbo Boost frequency is dependent on the number of active cores and varies by processor line item configuration. Intel® TBT can be enabled or disabled via BIOS. It is highly recommended that the Voltage Regulator IMON linearity and accuracy be maximized for best possible performance while in Turbo Boost.

8.5 Enhanced Intel SpeedStep® Technology

The processor features Enhanced Intel SpeedStep® Technology. Following are the key features of Enhanced Intel SpeedStep Technology:

- Multiple voltage and frequency operating points provide optimal performance at the lowest power.
- Voltage and frequency selection is software controlled by writing to processor MSRs:
  - If the target frequency is higher than the current frequency, V_{CC} is ramped up in steps by placing new values on the VID pins and the PLL then locks to the new frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the new frequency and the V_{CC} is changed through the VID pin mechanism.
  - Software transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition completes.
- The processor controls voltage ramp rates internally to ensure smooth transitions.
- Low transition latency and large number of transitions possible per second:
  - Processor core (including shared cache) is unavailable for less than 2 µs during the frequency transition.

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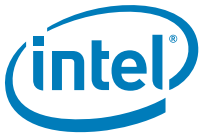


9 Boxed Processor Specifications

9.1 Introduction

Intel boxed processors are intended for system integrators who build systems from components available through distribution channels. The Intel® Xeon® processor 5600 series will be offered as an Intel boxed processor, however the thermal solution will be sold separately.

Intel Xeon processor 5600 series boxed processors will not include a thermal solution in the box. Intel will offer boxed thermal solutions separately through the same distribution channels. Please reference Section 9.1.1 - Section 9.1.4 for more details on Boxed Processor Thermal Solutions.

9.1.1 Available Boxed Thermal Solution Configurations

Intel will offer three different Boxed Heat Sink solutions to support Boxed Processors.

- Boxed Intel® Thermal Solution STS100C (Order Code BXSTS100C): A Passive / Active Combination Heat Sink Solution that is intended for processors with a TDP up to 130W in a pedestal or 2U+ chassis with appropriate ducting.
- Boxed Intel® Thermal Solution STS100A (Order Code BXSTS100A): An Active Heat Sink Solution that is intended for processors with a TDP of 80W or lower in pedestal chassis.
- Boxed Intel® Thermal Solution STS100P (Order Code BXSTS100P): A 25.5 mm Tall Passive Heat Sink Solution that is intended for processors with a TDP of 95W or lower in Blades, 1U, or 2U chassis with appropriate ducting.

9.1.2 Intel Thermal Solution STS100C (Passive / Active Combination Heat Sink Solution)

The STS100C, based on a 2U passive heat sink with a removable fan, is intended for use with processors with TDP's up to 130W. This heat pipe-based solution is intended to be used as either a passive heat sink in a 2U or larger chassis, or as an active heat sink for pedestal chassis. Figure 9-1 and Figure 9-2 are representations of the heat sink solution. Although the active combination solution with the removable fan installed mechanically fits into a 2U keepout, its use has not been validated in that configuration.

The STS100C in the active fan configuration is primarily designed to be used in a pedestal chassis where sufficient air inlet space is present. The STS100C with the fan removed, as with any passive thermal solution, will require the use of chassis ducting and are targeted for use in rack mount or ducted pedestal servers. The retention solution used for these products is called Unified Retention System (URS).

Figure 9-1. STS100C Passive / Active Combination Heat Sink (with Removable Fan)

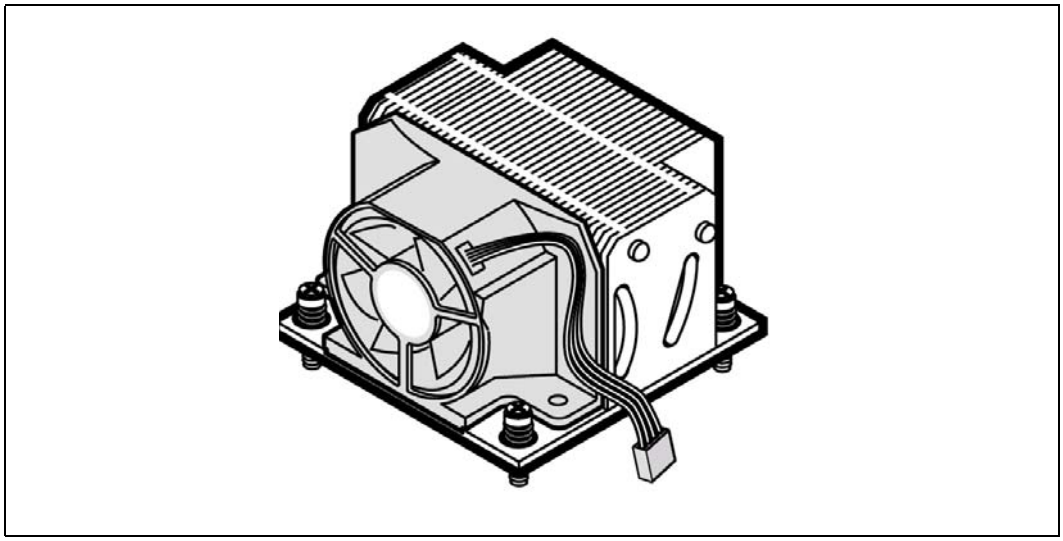
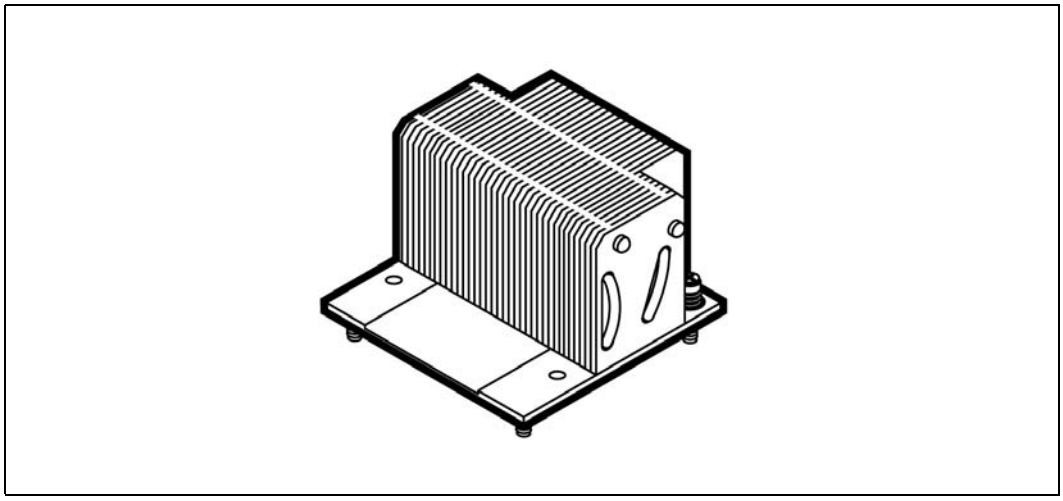


Figure 9-2. STS100C Passive / Active Combination Heat Sink (with Fan Removed)

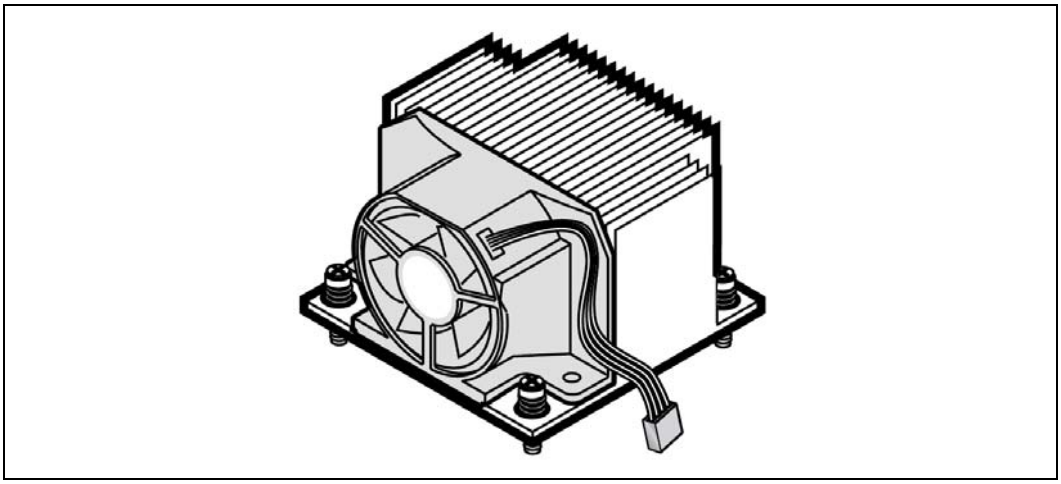


9.1.3 Intel Thermal Solution STS100A (Active Heat Sink Solution)

The STS100A will be available for purchase for processors with TDP's of 80W and lower and is an aluminum extrusion. This heat sink solution is intended to be used as an active heat sink only for pedestal chassis. Figure 9-3 is a representation of the heat sink solution.

The STS100C and STS100A utilize a fan capable of 4-pin pulse width modulated (PWM) control. Use of a 4-pin PWM controlled active thermal solution helps customers meet acoustic targets in pedestal platforms through the baseboard's ability to directly control the RPM of the processor heat sink fan. See Section 9.3 for more details on fan speed control. Also see Section 7.3 for more on the PWM and PECI interface along with Digital Thermal Sensors (DTS).

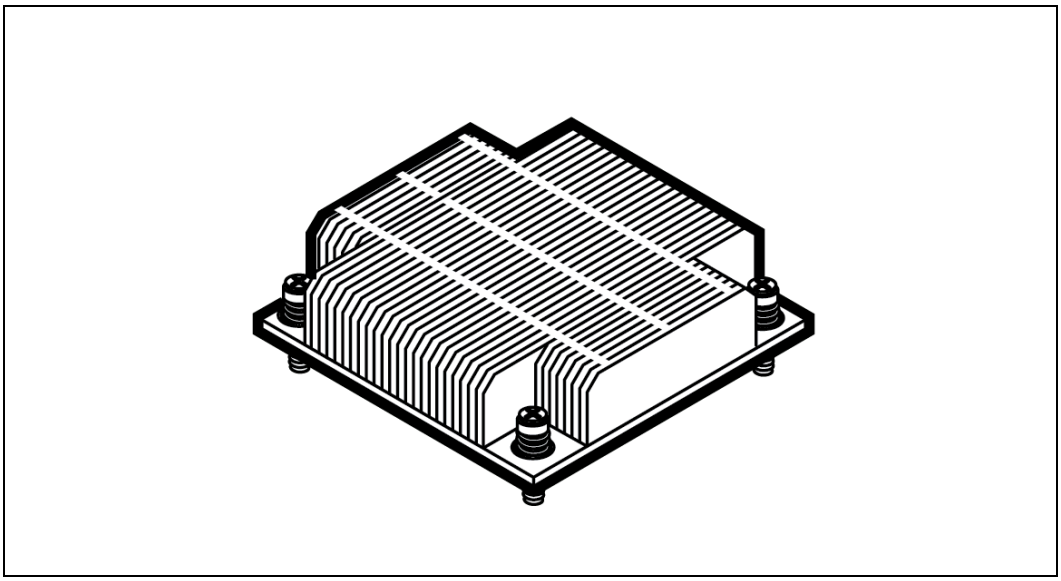
Figure 9-3. STS100A Active Heat Sink



9.1.4 Intel Thermal Solution STS100P (Boxed 25.5 mm Tall Passive Heat Sink Solution)

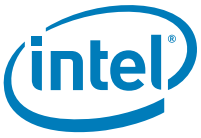
The STS100P is available for use with boxed processors that have TDP's of 95W and lower. The 25.5 mm Tall passive solution is designed to be used in SSI Blades, 1U, and 2U chassis where ducting is present. The use of a 25.5 mm Tall heatsink in a 2U chassis is recommended to achieve a lower heatsink T_{LA} and a more optimized heatsink design. Figure 9-4 is a representation of the heat sink solution. The retention solution used for these products is called Unified Retention System (URS).

Figure 9-4. STS100P 25.5 mm Tall Passive Heat Sink



9.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed processor solution.



9.2.1 Boxed Processor Heat Sink Dimensions and Baseboard Keepout Zones

The boxed processor and boxed thermal solutions will be sold separately. Clearance is required around the thermal solution to ensure unimpeded airflow for proper cooling. Baseboard keepout zones are shown in Figure 9-5 through Figure 9-7. Physical space requirements and dimensions for the boxed processor and assembled heat sink are shown in Figure 9-8 and Figure 9-9. Mechanical drawings for the 4-pin fan header and 4-pin connector used for the active fan heat sink solution are represented in Figure 9-11 and Figure 9-12.

None of the heat sink solutions exceed a mass of 550 grams. Note that this is per processor, a dual processor system will have up to 1100 grams total mass in the heat sinks.

See Section 4 for details on the processor mass.

Figure 9-5. Top Side Baseboard Keep-Out Zones

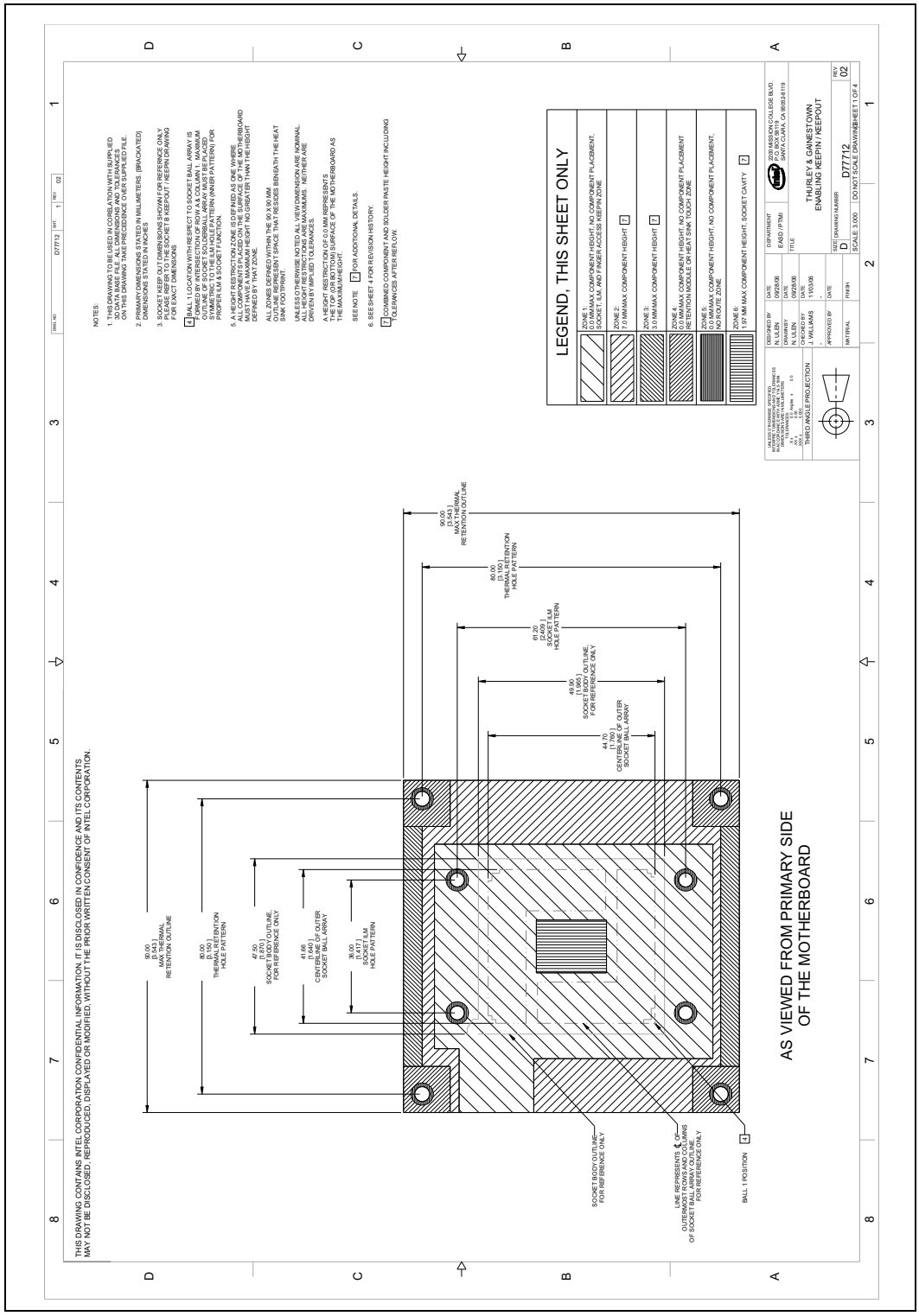


Figure 9-6. Top Side Baseboard Mounting-Hole Keep-Out Zones

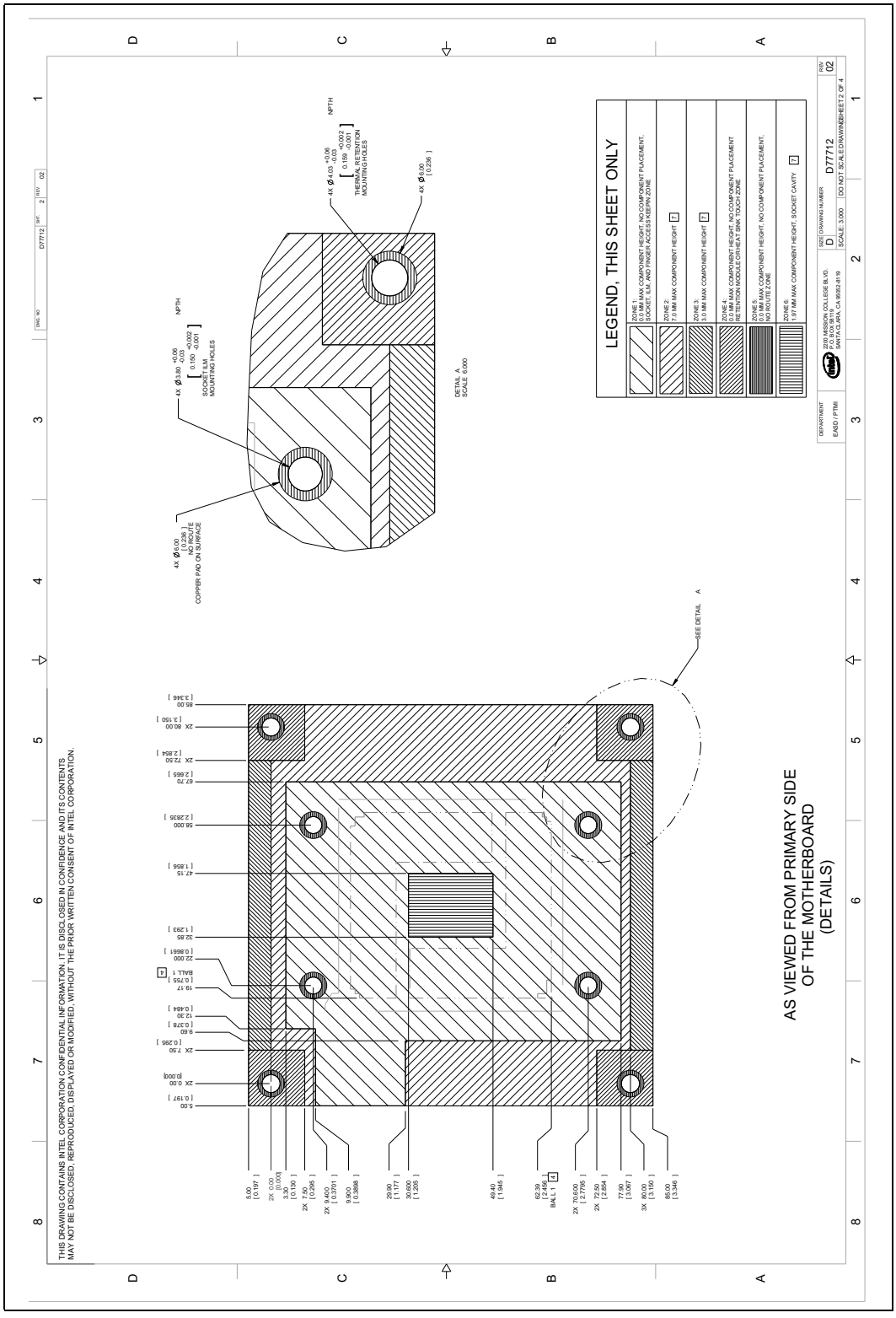


Figure 9-7. Bottom Side Baseboard Keep-Out Zones

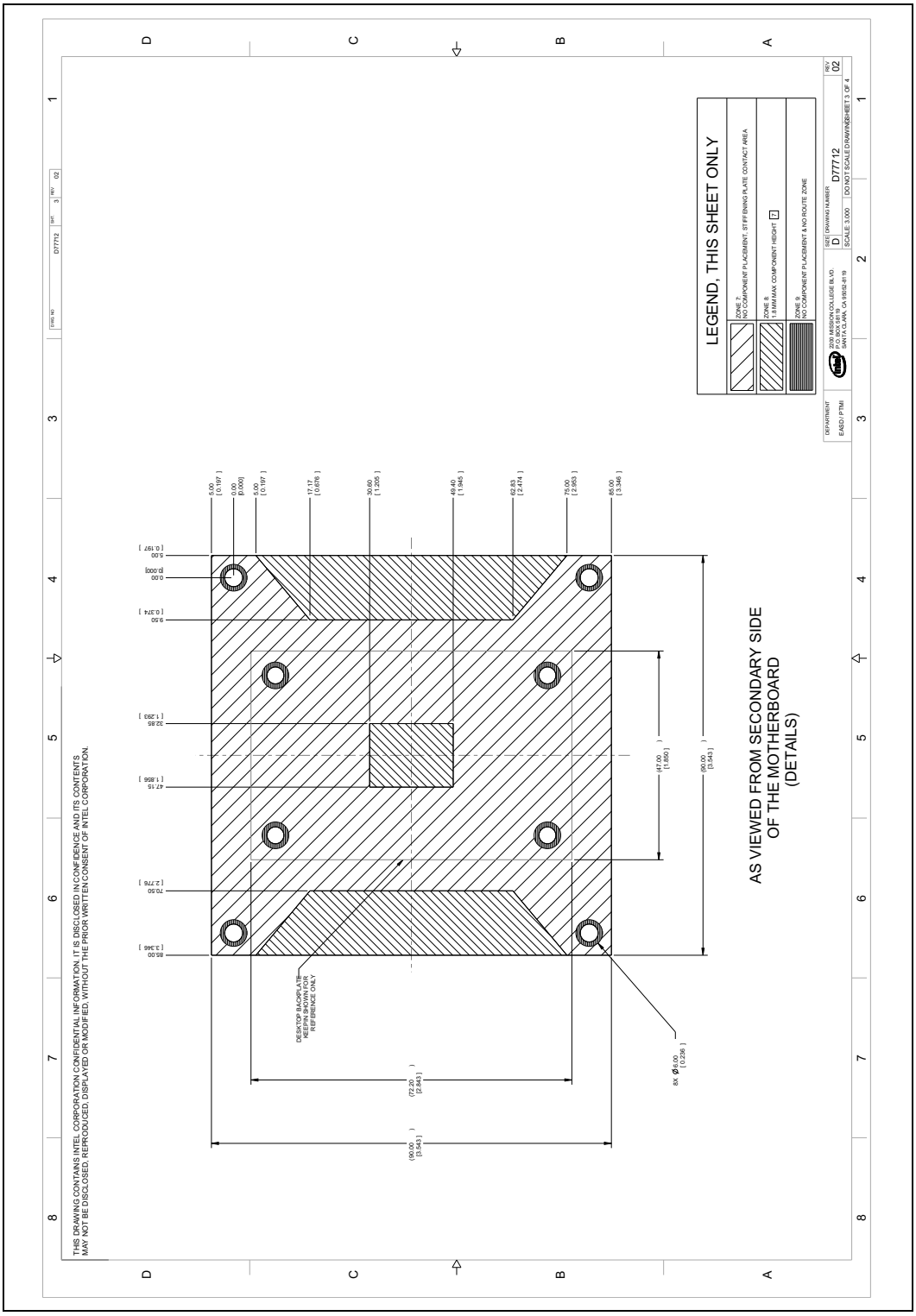


Figure 9-8. Primary and Secondary Side 3D Height Restriction Zones

Figure 9-9. Volumetric Height Keep-Ins

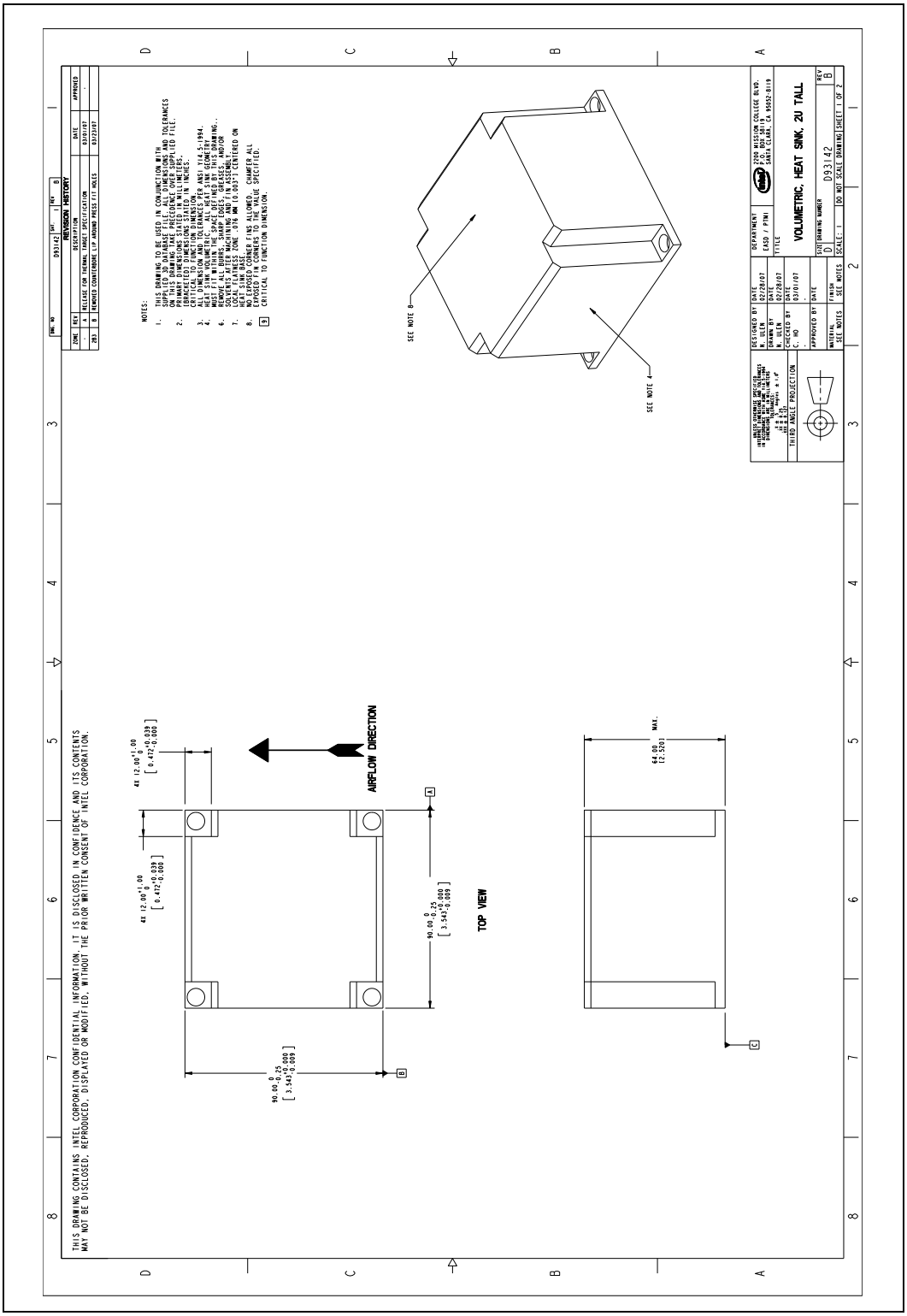


Figure 9-10. Volumetric Height Keep-Ins

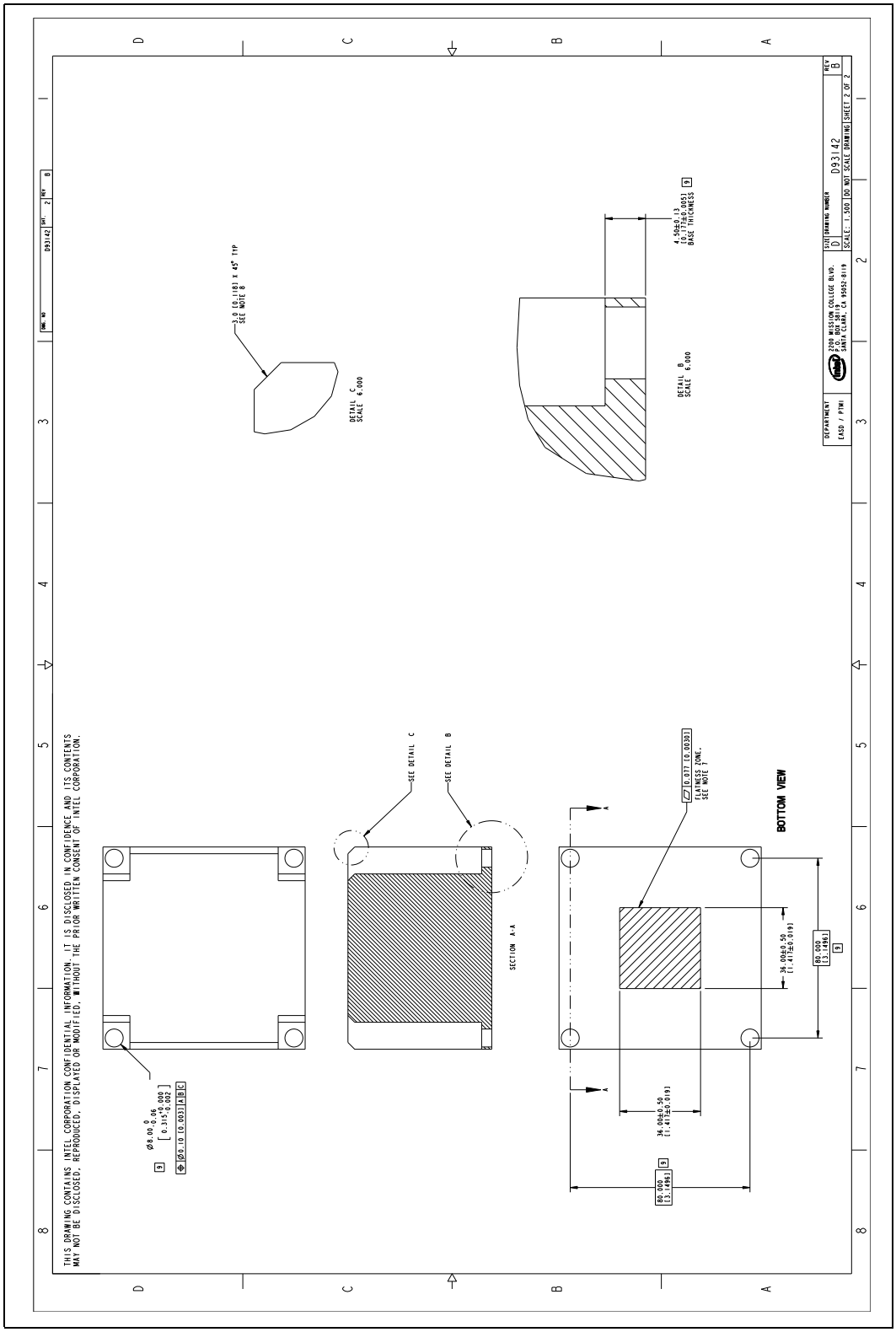


Figure 9-11. 4-Pin Fan Cable Connector (For Active Heat Sink)

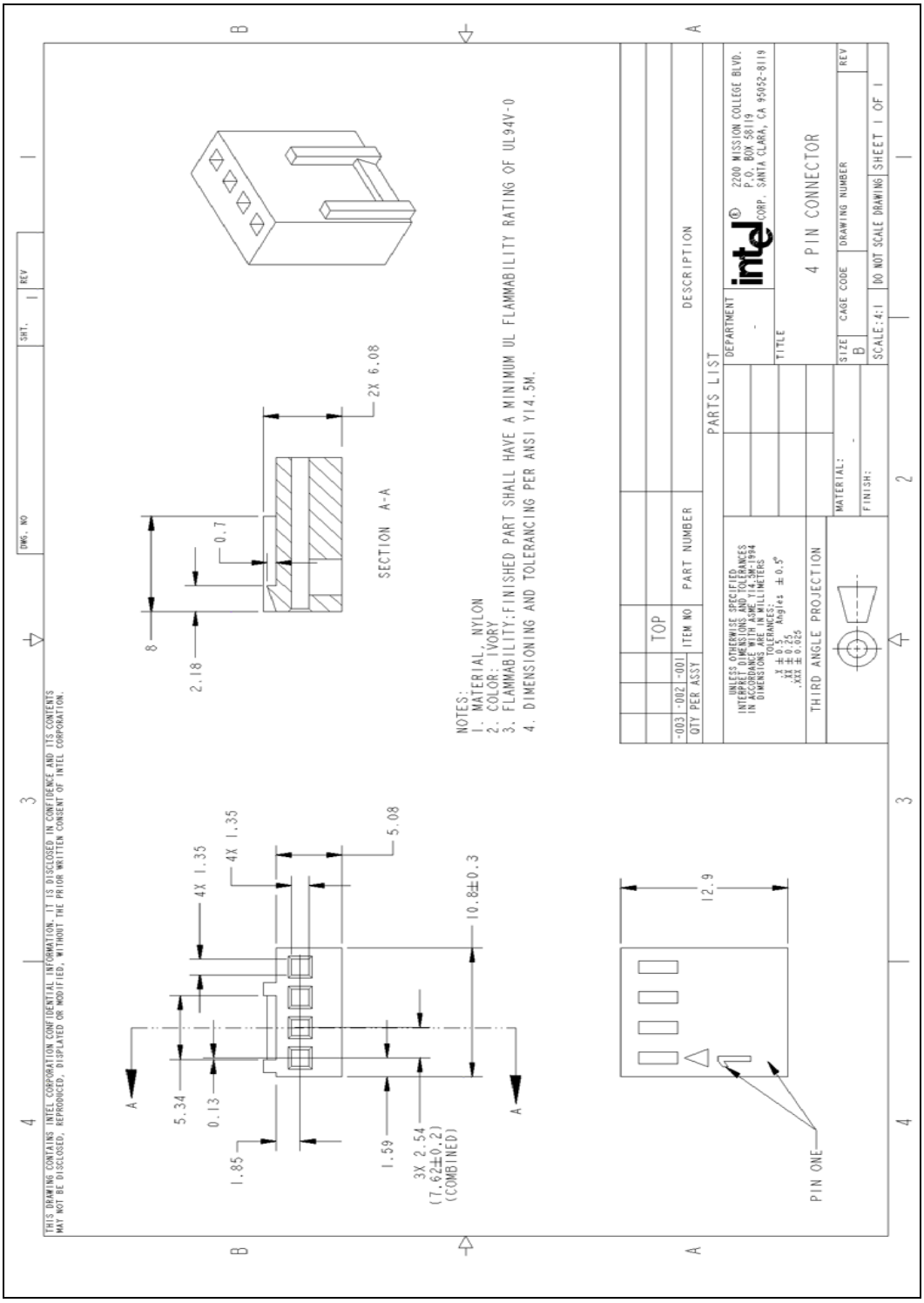
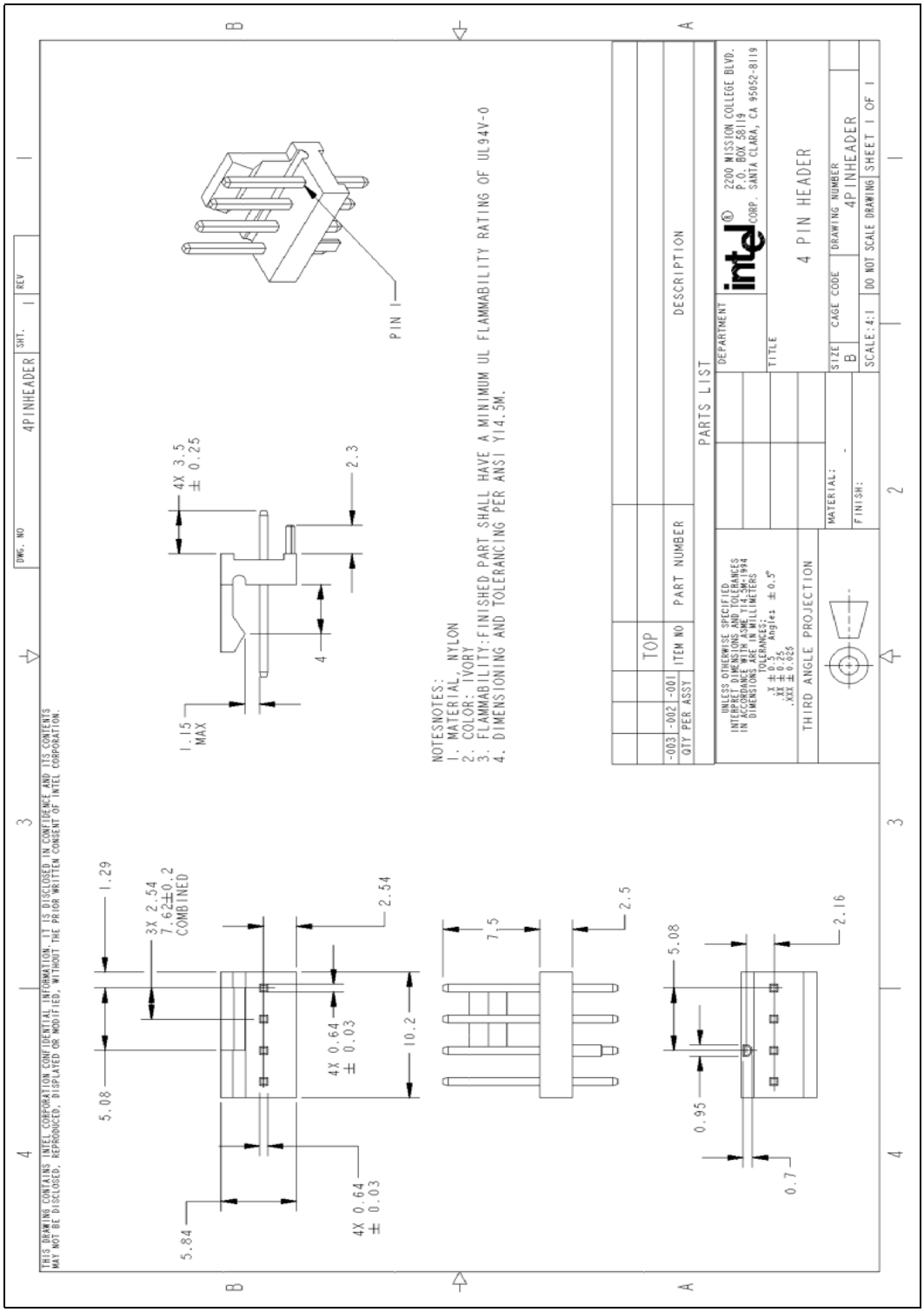
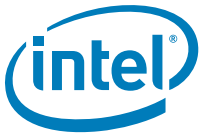


Figure 9-12. 4-Pin Base Baseboard Fan Header (For Active Heat Sink)





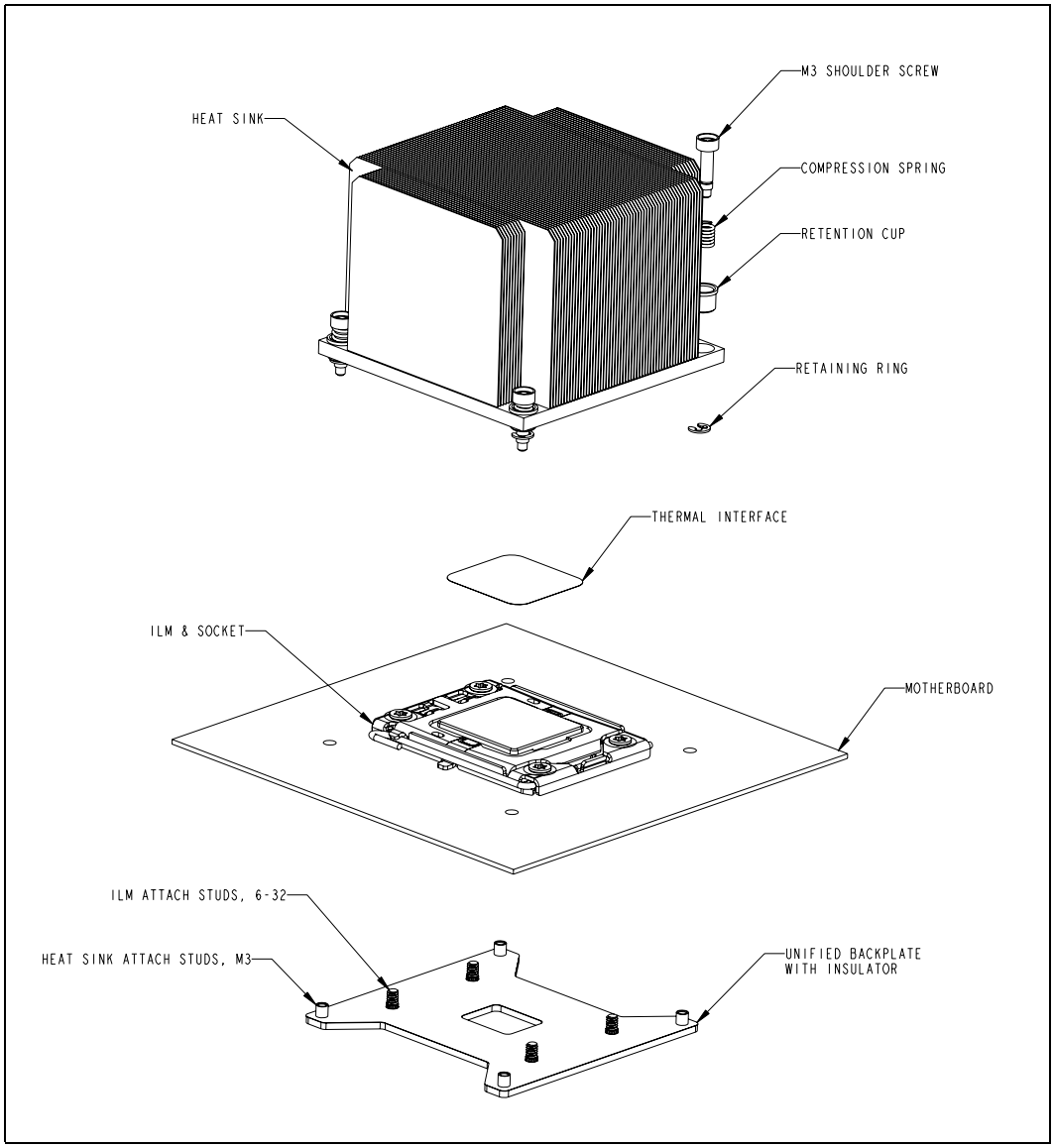
9.2.2 Boxed Processor Retention Mechanism and Heat Sink Support (URS)

Baseboards designed for use by a system integrator should include holes that are in proper alignment with each other to support the boxed processor. Refer to Figure 9-5 and Figure 9-5 for mounting hole dimensions.

Figure 9-13 illustrates the Unified Retention System (URS) and the Unified Backplate Assembly. The URS is designed to extend air-cooling capability through the use of larger heat sinks with minimal airflow blockage and bypass. URS retention transfers load to the baseboard via the Unified Backplate Assembly. The URS spring, captive in the heatsink, provides the necessary compressive load for the thermal interface material.

All components of the URS heat sink solution will be captive to the heat sink and will only require a Phillips screwdriver to attach to the Unified Backplate Assembly. When installing the URS the screws should be tightened until they will no longer turn easily. This should represent approximately 8 inch-pounds of torque. More than that may damage the retention mechanism components.

Figure 9-13. Thermal Solution Installation



Note: Actual boxed thermal solution may differ from this image, but installation is similar.

9.3 Fan Power Supply [STS100C (Combo) and STS100A (Active) Solutions]

The 4-pin PWM controlled thermal solution is being offered to help provide better control over pedestal chassis acoustics. This is achieved though more accurate measurement of processor die temperature through the processor's Digital Thermal Sensors. Fan RPM is modulated through the use of an ASIC located on the baseboard that sends out a PWM control signal to the 4th pin of the connector labeled as Control. This thermal solution requires a constant +12 V supplied to pin 2 of the active thermal

solution and does not support variable voltage control or 3-pin PWM control. See Figure 9-14 and Table 9-1 through Table 9-3 for details on the 4-pin active heat sink solution connectors.

The fan power header on the baseboard must be positioned to allow the fan heat sink power cable to reach it. The fan power header identification and location must be documented in the suppliers platform documentation, or on the baseboard itself. The baseboard fan power header should be positioned within 177.8 mm [7 in.] from the center of the processor socket.

Table 9-1. PWM Fan Frequency Specifications For 4-Pin Active Thermal Solution

Description	Min Frequency	Nominal Frequency	Max Frequency	Unit
PWM Control Frequency Range	21,000	25,000	28,000	Hz

Table 9-2. Fan Specifications For 4-Pin Active Thermal Solution

Description	Min	Typ Steady	Max Steady	Max Startup	Unit
+12 V: 12 volt fan power supply	10.8	12	12	13.2	V
IC: Fan Current Draw	N/A	1.25	1.5	2.2	A
SENSE: SENSE frequency	2	2	2	2	Pulses per fan revolution

Figure 9-14. Fan Cable Connector Pin Out For 4-Pin Active Thermal Solution

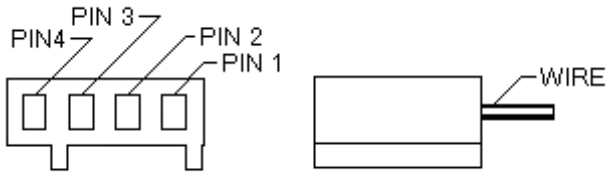


Table 9-3. Fan Cable Connector Pin Out for 4-Pin Active Thermal Solution

Pin Number	Signal	Color
1	Ground	Black
2	**Power:** (+12 V)	Yellow
3	**Sense:** 2 pulses per revolution	Green
4	**Control:** 21 kHz-28 kHz	Blue

9.3.1 Boxed Processor Cooling Requirements

As previously stated the boxed processor will have three cooling solutions available. Each configuration will require unique design considerations. Meeting the processor's temperature specifications is also the function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specifications are found in Section 7 of this document.

9.3.1.1 STS100C (Passive / Active Combination Heat Sink Solution)

Active Configuration:

The active configuration of the combination solution is designed to help pedestal chassis users to meet the thermal processor requirements without the use of chassis ducting. It may be still be necessary to implement some form of chassis air guide or air duct to meet the T_{LA} temperature of 40 °C depending on the pedestal chassis layout. Use of the active configuration in a 2U rackmount chassis is not recommended.

It is recommended that the ambient air temperature outside of the chassis be kept at or below 35 °C. The air passing directly over the processor thermal solution should not be preheated by other system components. Meeting the processor's temperature specification is the responsibility of the system integrator.

This thermal solution is for use with 95 W and 130 W TDP processor SKUs.

Passive Configuration:

In the passive configuration it is assumed that a chassis duct will be implemented. Processors with a TDP of 130W or 95W must provide a minimum airflow of 30 CFM at 0.205 in. H_2O (51 m^3/hr at 51.1 Pa) of flow impedance. For processors with a TDP of 130W it is assumed that a 40 °C T_{LA} is met. This requires a superior chassis design to limit the T_{RISE} at or below 5°C with an external ambient temperature of 35°C. For processors with a TDP of 95W it is assumed that a 55 °C T_{LA} is met.

9.3.1.2 STS100A (Active Heat Sink Solution) (Pedestal only)

This active solution is designed to help pedestal chassis users to meet the thermal processor requirements without the use of chassis ducting. It may be still be necessary to implement some form of chassis air guide or air duct to meet the T_{LA} temperature of 40°C depending on the pedestal chassis layout. Use of this active solution in a 2U rackmount chassis has not been validated.

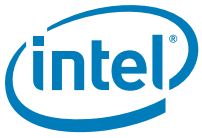
It is recommended that the ambient air temperature outside of the chassis be kept at or below 35 °C. The air passing directly over the processor thermal solution should not be preheated by other system components. Meeting the processor's temperature specification is the responsibility of the system integrator.

This thermal solution is for use with processor SKUs no higher than 80 W.

9.3.1.3 STS100P (25.5 mm Tall Passive Heat Sink Solution) (Blade + 1U + 2U Rack)

This passive solution is intended for use in SSI Blade, 1U or 2U rack configurations. It is assumed that a chassis duct will be implemented in all configurations.

Processors with a TDP of 95 W must provide a minimum airflow of 16 CFM at 0.40 in. H2O (27.2 m3/hr at 99.5 Pa) of flow impedance. It is assumed that a TLA of 49°C is met for 95 W processor installations. This requires a chassis design to limit the TRISE at or below 14°C with an external ambient temperature of 35°C. Under these conditions, only Thermal Profile B will be supported. If Thermal Profile A support is desired for processors with a TDP of 95 W a 2U configuration with a chassis duct is recommended. A TLA of <40°C is required. This requires a superior chassis design to limit the TRISE below 5°C with an external ambient temperature of 35°C.



Processors with a TDP of 80 W or lower must provide a minimum airflow of 9.7 CFM at 0.20 in. H2O (16.5 m3/hr at 49.8 Pa) of flow impedance. It is assumed that a TLA of 49°C is met for these processor installations. This requires a chassis design to limit the TRISE at or below 14°C with an external ambient temperature of 35°C.

Note: lease refer to the *Intel® Xeon® Processor 5500/5600 Series Thermal / Mechanical Design Guidelines* for detailed mechanical drawings of the STS100P.

9.4 Boxed Processor Contents

The Boxed Processor and Boxed Thermal Solution contents are outlined below.

Boxed Processor

- Intel® Xeon® processor 5600 series processor
- Installation and warranty manual
- Intel Inside Logo

Boxed Thermal Solution

- Heat sink assembly solution
- Thermal interface material (pre-applied on heat sink, if included)
- Installation and warranty manual

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