AN-EVALSF3-ICE3AS03LJG

65W 19.5V SMPS Evaluation Board with F3 PWM controller ICE3AS03LJG

Power Management & Supply

Never stop thinking.

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65W 19.5V Demo board using ICE3AS03LJG on board

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65W 19.5V SMPS Evaluation Board with F3 PWM controller ICE3AS03LJG:
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Table of Contents Page

1 Abstract

This document is an engineering report that describes a universal input power supply designed in a 19.5V 65W off line flyback converter that utilizes the F3 PWM controller ICE3AS03LJG. The application board is operated in discontinuous current mode and running at 100 kHz switching frequency. It has one output voltage with secondary side control regulation. It is especially suitable for AC/DC power supply such as LCD monitors, adapters for printers and notebook computers, DVD players and recorder, Blue-Ray DVD player and recorder, set-top boxes and industrial auxiliary power supplies. The ICE3AS03LJG is a current mode PWM controller. With the 500V startup cell, active burst mode and BiCMOS technologies, the standby power can be <100mW at no load. The frequency jitter mode and the soft gate drive can give a low EMI performance. The built-in 20ms blanking window and the extendable blanking time approach can prevent the IC from entering the auto restart mode due to over load protection unintentionally. The outstanding propagation delay compensation feature can allow a very precise current limit between low line and high line. For this IC, it provides both auto-restart and latch off protection mode. For those serious faults such as Vcc over-voltage, over temperature, short transformer winding, etc, the IC will enter the latched off protection mode. For those less severe case such as the over load, open loop, short opto-coupler, etc, it enters the auto restart protection mode. In case it needs customer defined protection, the external latch off enable feature can fulfill the requirement. By using this feature, an external over temperature protection circuit for the MOSFET is implemented in this evaluation board.

2 Evaluation Board

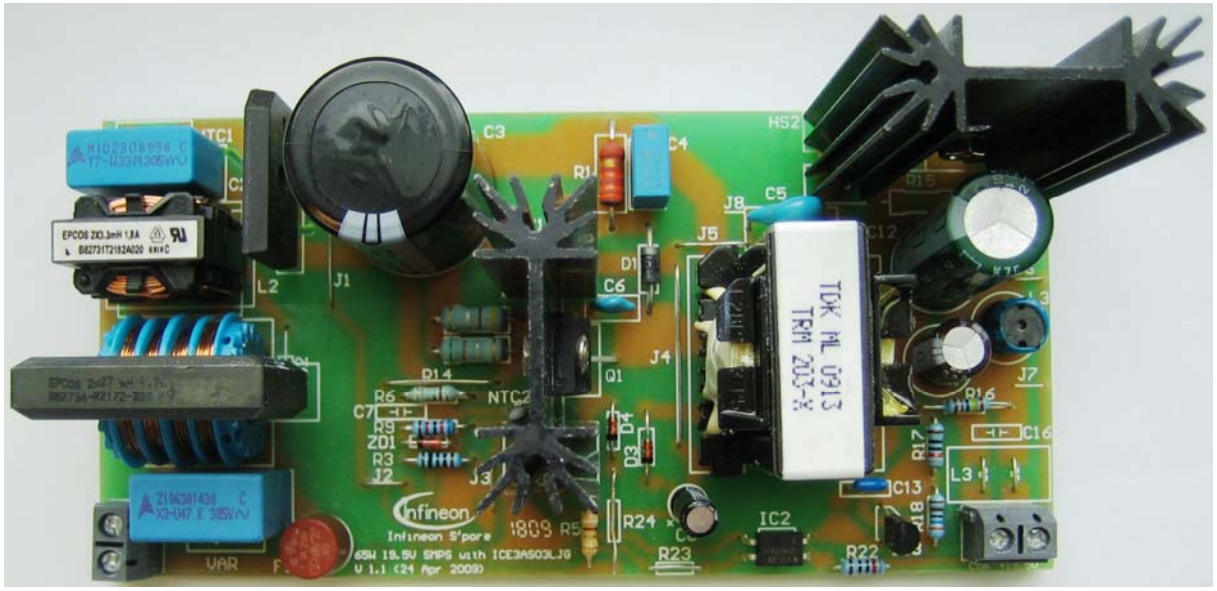

Figure 1a – EVALSF3-ICE3AS03LJG (top view)

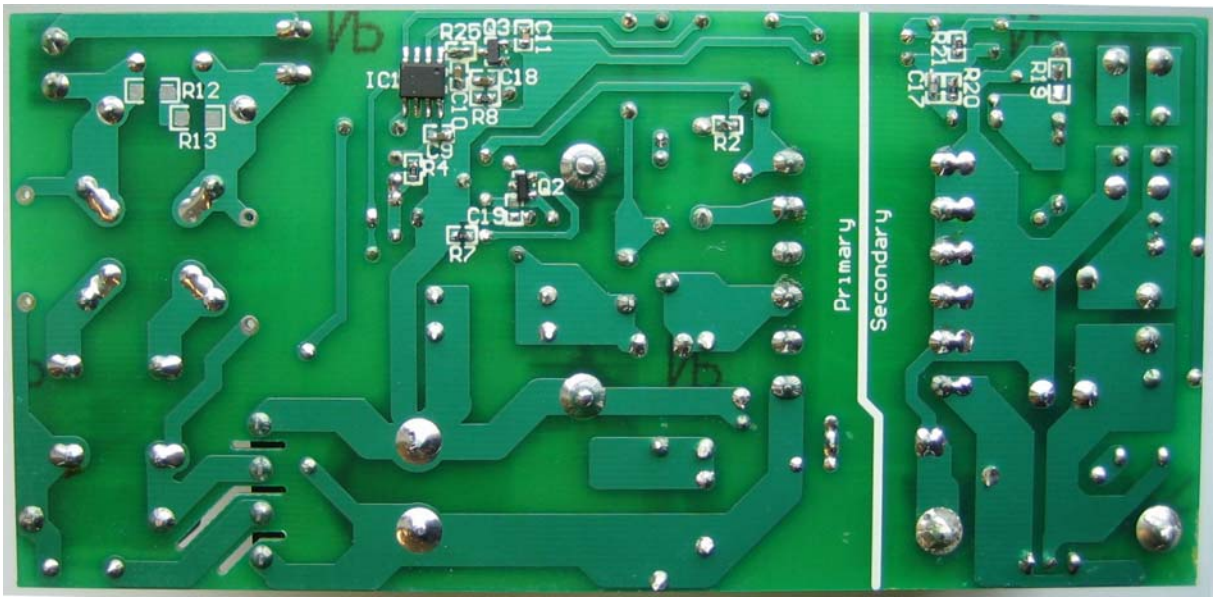

Figure 1b – EVALSF3-ICE3AS03LJG (bottom view)

This document contains the list of features, the power supply specification, schematic, bill of material and the transformer construction drawing. Typical operating characteristics and performance curves with scope waveforms are presented at the rear of the report.

3 List of Features

500V Startup Cell switched off after Start Up
Active Burst Mode for lowest Standby Power
Fast load jump response in Active Burst Mode
100kHz internally fixed switching frequency
Built-in Latched Off Protection Mode for Overtemperature, Overvoltage & Short Winding
Built-in Auto Restart Protection Mode for Overload, Open Loop,VCC Undervoltage & Short Optocoupler
Built-in Soft Start
Built-in blanking window with extendable blanking time for short duration high current
External latch off enable function
Max Duty Cycle 75%
Overall tolerance of Current Limiting < ±5%
Internal PWM Leading Edge Blanking
BiCMOS technology provide wide VCC range
Frequency jitter and soft gate driving for low EMI

4 Technical Specifications

Input voltage	85VAC~265VAC
Input frequency	50Hz, 60Hz
Input Standby Power	< 100mV @ no load; < 1W @ 0.5W load
Output voltage and current	19.5V +/- 2%
Output current	3.34A
Output power	65W
Average Efficiency	>85% (115Vac & 230Vac)
Output ripple voltage	< 130mVp-p

5 Circuit Diagram

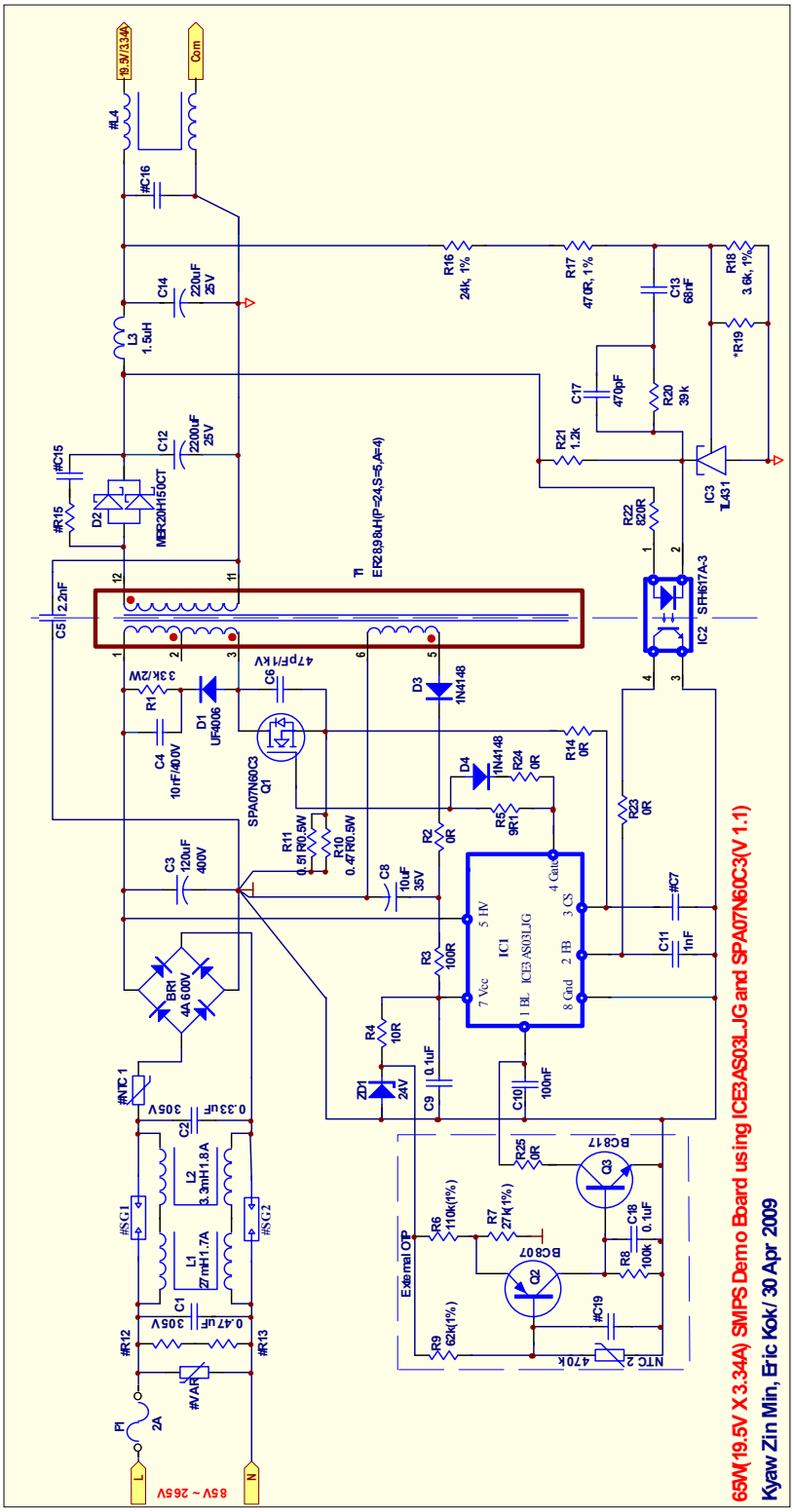

Figure 2 – 65W 19.5V ICE3AS03LJG power supply schematic

N.B.: In order to get the optimized performance of the PWM controller, the grounding of the PCB layout must be taken very carefully. From the circuit diagram above, it shows that the grounding for the PWM controller can be split into several groups; signal ground, Vcc ground and Current sense resistor ground. All the split ground should be connected to the bulk capacitor ground directly.

- Signal ground includes all small signal grounds connecting to the PWM controller GND pin such as filter capacitor ground of C9, C10, C11, C7 and opto-coupler ground.
- Vcc ground includes the Vcc capacitor ground, C8 and the auxiliary winding ground; pin 6 of the power transformer.
- Current Sense resistor ground includes current sense resistor R10 and R11.

6 PCB Layout

6.1 Component side component legend

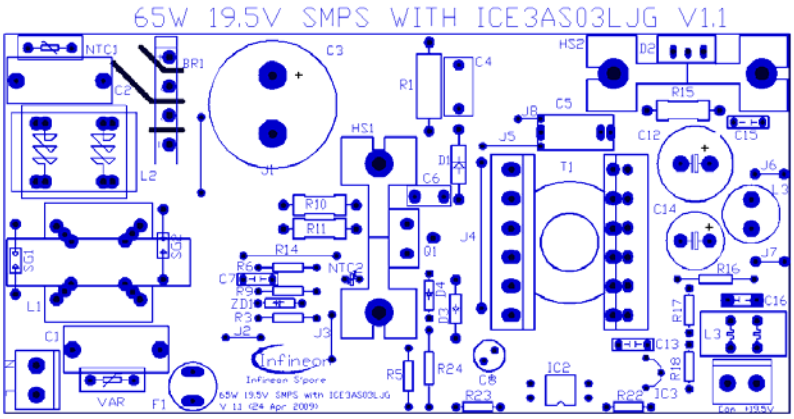

Figure 3 – Component side Component Legend – View from Component Side

6.2 Solder side copper & component legend

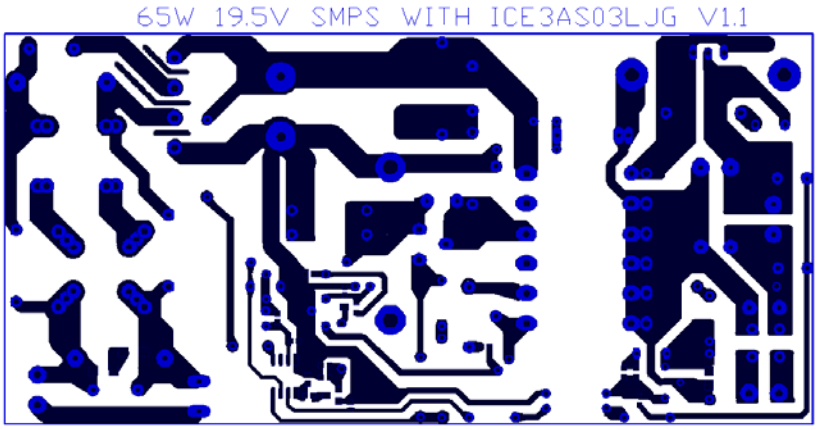

Figure 4a – Solder side copper – View from Component Side

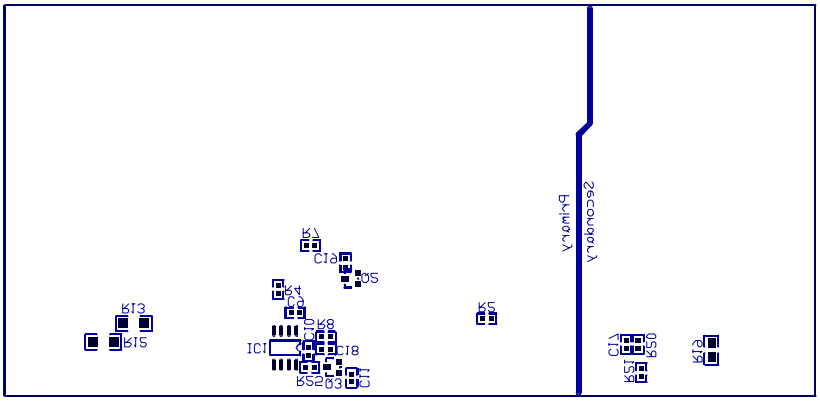

Figure 4b – Solder side component legend – View from Component Side

7 Circuit Description

7.1 Introduction

The EVALSF3-ICE3AS03LJG demo board is an off line flyback switch mode power supply (SMPS) using the ICE3AS03LJG PWM IC from the Infineon PWM controller. The circuit, shown in Figure 2, details a 19.5V, 65W power supply that operates from an AC line input voltage range of 85Vac to 265Vac, suitable for applications requiring either an open frame supply or an enclosed adapter.

7.2 Line Input

The AC input side comprises the input fuse F1 as over-current protection. The common mode choke L1 and L2, X2-capacitors C1 and C2 and Y1-capacitor C5 act as EMI suppressors. A varistor VAR (optional) is added to absorb the line transient while a NTC1 (optional) is added to reduce the inrush surge current during start up. Two series resistor, R12 and R13 (optional) are added to discharge the voltage at C1 and C2 after the AC line is removed. A rectified DC voltage (120V ~ 375V) is obtained through the bridge rectifier BR1 and the input bulk capacitor C3.

7.3 Start up

Since there is a built-in startup cell in the ICE3AS03LJG, there is no need for external start up resistors. The startup cell is connecting the HV pin of the IC. Once the voltage is built up at the HV pin of the ICE3AS03LJG, the startup cell will charge up the Vcc capacitor C8 and C9. When the Vcc voltage exceeds the UVLO at 18V, the IC starts up. Then the Vcc voltage is bootstrapped by the auxiliary winding to sustain the operation.

7.4 Operation mode

During operation, the Vcc pin is supplied via a separate transformer winding with associated rectification D3 and buffering and filtering capacitors C8 and C9. Resistor R2 and R3 are used for current limiting. In order not to exceed the maximum voltage at Vcc pin, an external zener diode ZD1 and R4 is added to clamp the voltage.

7.5 Soft start

The Soft-Start time is built-in 10ms. After the Vcc hits UVLO at 18V, it starts the soft-start phase.

7.6 RCD Clamper circuit

While turning off the switch Q1, the clamper circuit R1, C4 and D1 absorbs the current caused by transformer leakage inductance once the voltage exceeds clamper circuit voltage. Then drain to source voltage is well below the maximum break down voltage.

7.7 Main switcher

Q1 is the main switcher for the system. It has a low Rdson to reduce the conduction loss. An optional drain-source capacitor C6 can be added to the MOSFET to reduce the switching noise so as to get a better EMI performance.

7.8 Gate drive

The gate drive current is 0.17A push and 0.39A pull. The gate on signal has installed with a slope controlled rising edge feature which make the driving softly. If it needs to optimize the EMI performance, a turn off resistor-diode network (R24 and D4) can be added in parallel with the gate drive resistor (R5) so as to turn the device off faster than it is turned on.

7.9 Peak current control of primary current

The power MOSFET drain source current is sensed via external shunt resistors R10 and R11 which determine the tolerance of the current limit control. Since ICE3AS03LJG is a current mode controller, it would have a cycle-by-cycle primary current and feedback voltage control which can make sure the maximum power of the converter is controlled in every switching cycle. Besides, propagation delay compensation is implemented to ensure the maximum input current/power can be controlled in an even tighter manner. The demo board shows app. +/-3.6% (refer to Figure 13).

7.10 Output Stage

The power is coupled to the secondary side through schottky diode D2. The capacitor C12 provides energy buffering and the cascading LC filter L2 and C14 is used to reduce the output voltage ripple. The capacitor C12 is selected to have a low internal resistance (ESR) to minimize the output voltage ripple.

7.11 Feedback and regulation

The output voltage is controlled by a TL431 reference control IC (IC3). This device incorporates the voltage reference as well as the error amplifier. Compensation network C13, C17, R16, R17, R18, R19 and R20 constitutes the loop compensation circuit. This circuitry allows the feedback to be precisely matched to dynamically varying load conditions and provides stable control. The maximum current through the optocoupler diode and the voltage reference is set by using resistors R21 and R22. Optocoupler IC2 is used to transmit the control signal to the “Feedback” input of the ICE3AS03LJG device. The selected optocoupler should meet DIN VDE 884 requirements for a wider creepage distance.

7.12 Blanking Window for Load Jump

In case of Load Jumps the Controller provides a Blanking Window before activating the Over Load Protection and entering the Auto Restart Mode. There are 2 modes for the blanking time setting; basic mode and the extendable mode. If there is no capacitor added to the BL pin, it would fall into the basic mode; i.e. the blanking time is set at 20ms. If a longer blanking time is required, a capacitor, C10 can be added to BL pin to extend it. The extended time can be achieved by an internal 13uA constant current at BL pin to charge C10 from 0.9V to 4.0V. Thus the overall blanking time is the addition of 20ms and the extended time. For example, C10 (external capacitor at BL pin) = 0.22uF, I_{BK} (internal charging current) = 13uA

Blanking time (total) = 20ms + C10 X (4-0.9)/I_{BK} = 72.5ms

Note: A filter capacitor (e.g. 100pF) may be needed to add to the BL pin if the noises cannot be avoided to enter that pin in the physical PCB layout. Otherwise, some protection features may be mis-triggered and the system may not be working properly.

7.13 Active Burst Mode

At light load condition, the SMPS enters into Active Burst Mode. At this stage, the controller is always active but the V_{CC} must be kept above the switch off threshold; i.e. $V_{CCoff} \geq 10.5V$. During active burst mode, the efficiency increases significantly and at the same time it supports low ripple on V_{OUT} and fast response on load jump. When the voltage level at FB falls below 1.23V, the internal blanking timer starts to count. When it reaches the built-in 20ms blanking time, it will enter Active Burst Mode. The Blanking Window is generated to avoid sudden entering of Burst Mode due to load jump.

During Active Burst Mode the current sense voltage limit is reduced from 1V to 0.25V so as to reduce the conduction losses and audible noise. All the internal circuits are switched off except the reference and bias voltages to reduce the total V_{CC} current consumption to below 0.45mA. At burst mode, the FB voltage is changing like a sawtooth between 3.0 and 3.5V. To leave Burst Mode, FB voltage must exceed 4.2V. It will reset the Active Burst Mode and turn the SMPS into Normal Operating Mode. The maximum current; i.e. current sense voltage limit resume to 1V, can then be provided to stabilize V_{OUT}.

7.14 Jitter mode

The ICE3AS03LJG has frequency jittering feature to reduce the EMI noise. The jitter frequency is internally set at 100 kHz (+/-4 kHz) and the jitter period is set at 4ms.

7.15 Protection modes

Protection is one of the major factors to determine whether the system is safe and robust. Therefore, sufficient protection is a must. ICE3AS03LJG provides all the necessary protections to ensure the system is operating safely. There are 2 kinds of protection mode; auto-restart and latch off mode. When there are serious faults such as Vcc over-voltage, over temperature and short winding, it enters the latch off mode. For those less severe faults such as over load, open loop, Vcc under-voltage and short optocoupler, it enters the auto-restart mode. In addition, there is an external latch enable feature which is suitable for those tailor-made protection features. An external OTP circuit is implemented to protect the MOSFET surface temperature at 110°C (heatsink temperature at 106°C). A list of protections and the failure conditions are showed in the below table.

Protection function	Failure condition	Protection Mode
Vcc Over-voltage	Vcc > 25.5V	Latch off
Over-temperature (controller junction)	T_J > 130°C	Latch off
Short winding / Short diode	V_{CS} > 1.66V	Latch off
External Latch off enable	V_{BL} < 0.33V	Latch off
Over-load / Open loop	V_{FB} > 4.2V and V_{BL} > 4.0V and after Blanking time	Auto Restart
Vcc Under-voltage / short Opto-coupler	Vcc < 10.5V	Auto Restart

8 Component List

No	Circuit code	Component description	Quantity	Manufacturer
1	BR1	4A 600V	1	Vishay
2	C1	0.47uF, 305V	1	EPCOS
3	C9,C10,C18	100nF,50V(0603)	3	
4	C11	1nF, 63V	1	Murata
5	C12	2200uF, 25V	1	
6	C13	68nF, 63V	1	Murata
7	C14	220uF, 25V	1	
8	C17	470pF, 50V(0603)	1	
9	C2	0.33uF, 305V	1	EPCOS
10	C3	120uF, 400V	1	EPCOS
11	C4	10nF, 400V	1	EPCOS
12	C5	2.2nF, 250V	1	Murata
13	C6	47pF, 1kV	1	Murata
14	C8	10uF, 35V	1	EPCOS
15	D1	UF4006	1	Vishay
16	D2	MBR20H150CT	1	Vishay
17	D3,D4	1N4148	2	Vishay
18	F1	2A 250V	1	
19	IC1	ICE3AS03LJG, SO-8	1	Infineon
20	IC2	SFH617 A3	1	Vishay
21	IC3	TL431	1	
22	J1 ~ J6,NTC1,R23,R24,R14,L3	Jumper	12	
23	L1	27mH, 1.7A	1	EPCOS
24	L2	3.3mH,1.8A	1	EPCOS
25	L3	1.5uH	1	NEC-Tokin
26	NTC2	470k(B57891M0474+000)	1	EPCOS
27	Q1	SPA07N60C3	1	Infineon
28	Q2	BC807-25	1	
29	Q3	BC817-25	1	
30	R1	33K, 2W	1	
31	R10	0.47R, 1/2W,1%	1	
32	R11	0.51R, 1/2W,1%	1	
33	R16	24k, 1%, 1/4W	1	
34	R17	470R, 1%, 1/4W	1	
35	R18	3.6k, 1%, 1/4W	1	
36	R2,R25	0R, 0603	2	
37	R20	39k,0603	1	
38	R21	1.2k, 0603	1	
39	R22	820R	1	
40	R3	100R, 1/4W	1	
41	R4	10R, (0603)	1	
42	R5	9R1, 1/4W	1	
43	R6	110k,1%	1	
44	R7	27k, (0603),1%	1	
45	R8	100k(0603)	1	
46	R9	62k,1%	1	
47	T1	98uH(P=24,S=5,A=4)	1	TDK
48	ZD1	24V	1	

9 Transformer Construction

Core and material: EER28L, PC47 or EER28/34/11, N72

Bobbin: EER28LEC P12 (Vertical type)

Primary Inductance, L_p = 98uH measured between pin 1 and pin 3 (Gapped to Inductance)

Transformer structure:

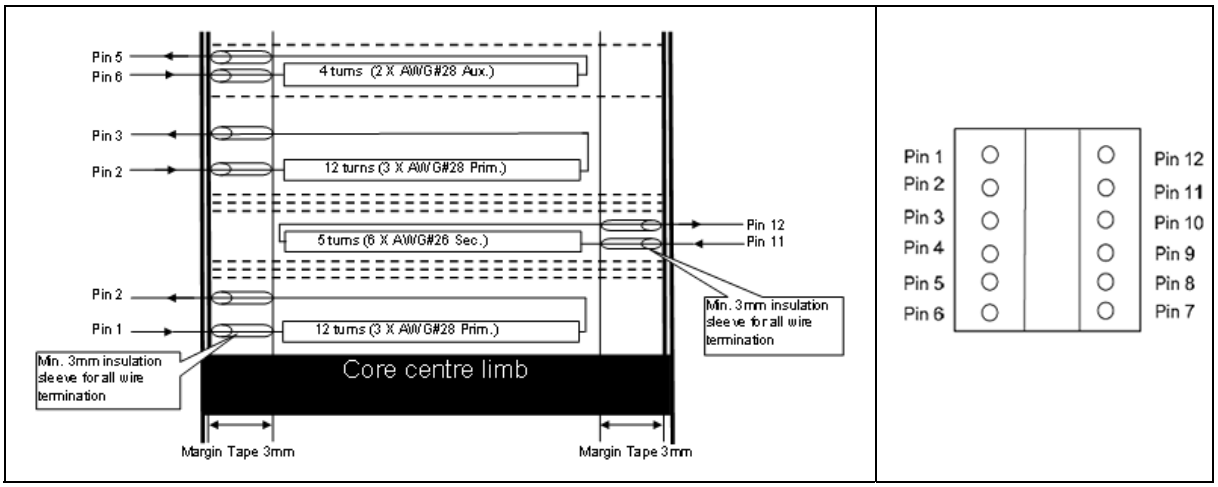

Figure 5 – Transformer structure and top view of transformer complete

Wire size requirement:

Start	Stop	No. of turns	Wire size	Layer
6	5	4	2XAWG#28	Aux.
2	3	12	3XAWG#28	$^1/_2$ Primary
11	12	5	6XAWG#26	Secondary
1	2	12	3XAWG#28	$^1/_2$ Primary

10 Test Results

10.1 Efficiency

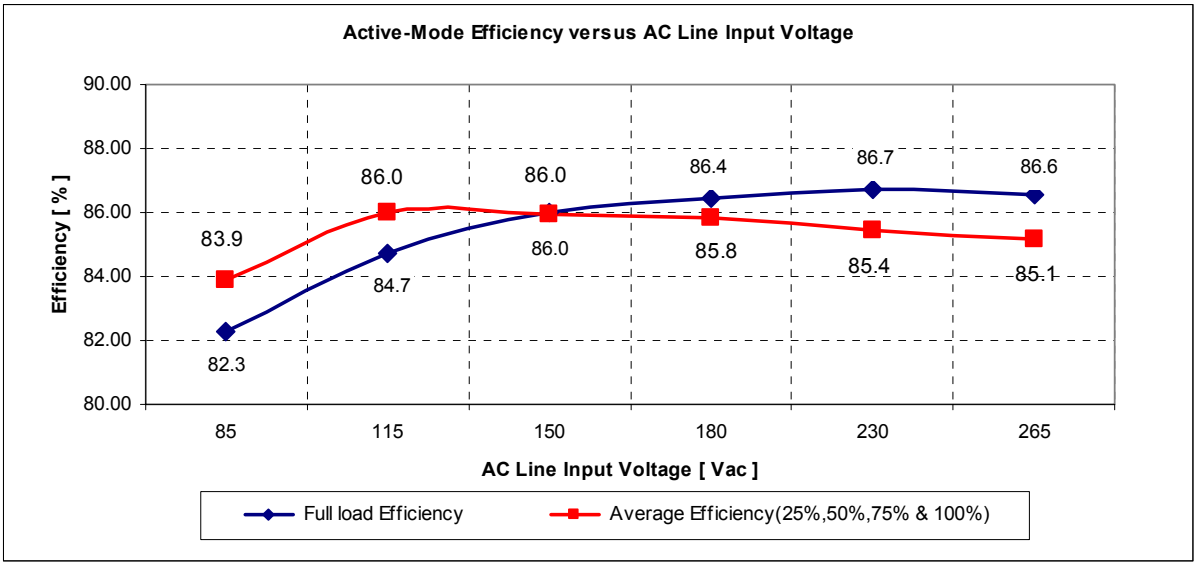

Figure 6 – Efficiency vs. AC Line Input Voltage

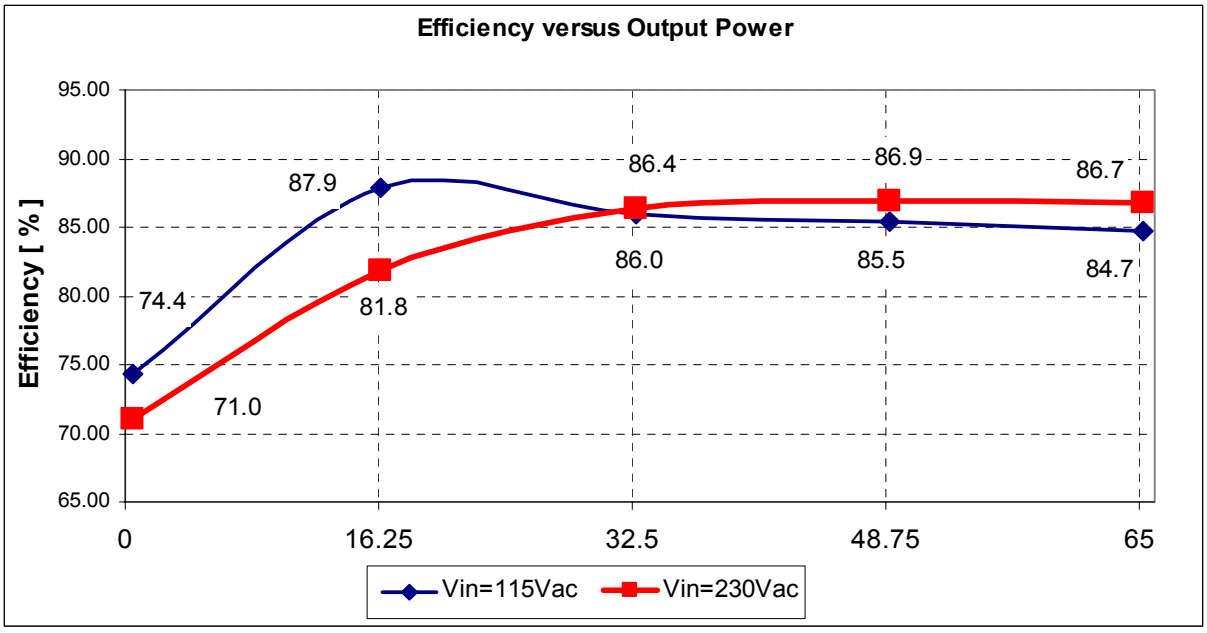

Figure 7 – Efficiency vs. Output Power @ Low and High Line

10.2 Input Standby Power

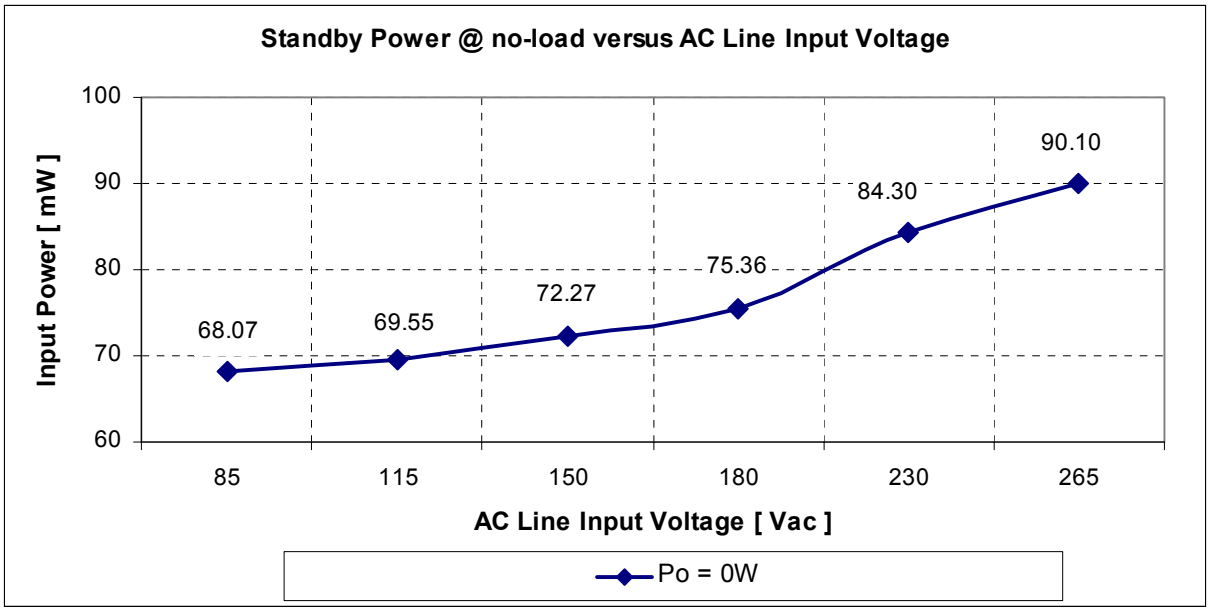

Figure 8 – Input Standby Power @ no load vs. AC Line Input Voltage
(Equipment: Yokogawa WT210 power meter – using integration mode)

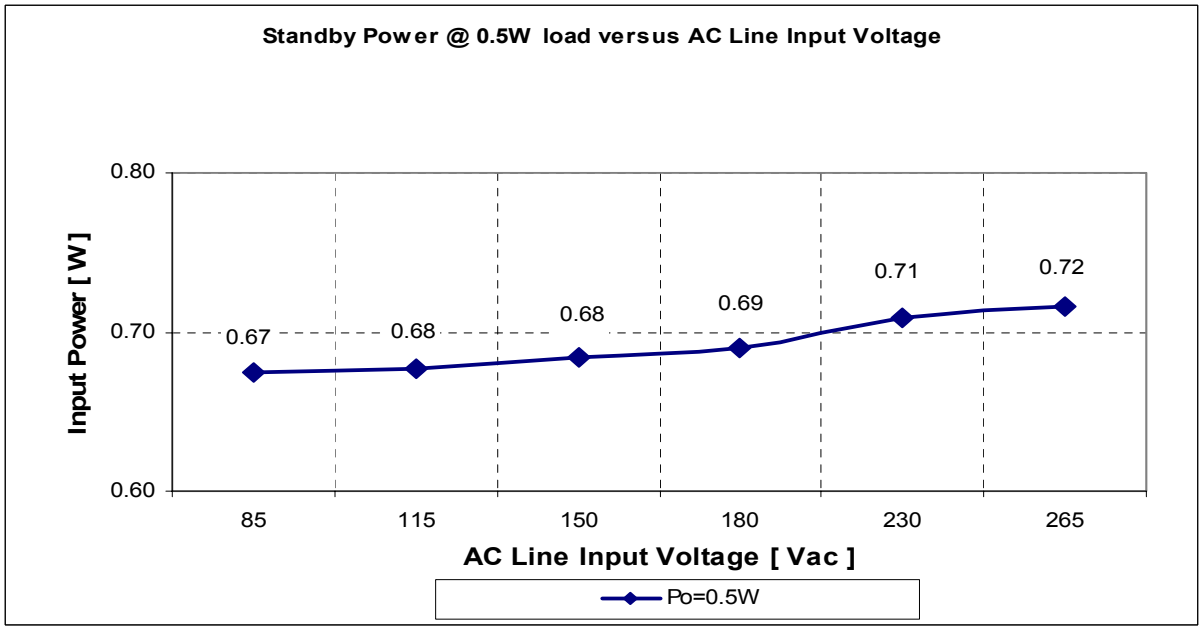

Figure 9 – Input Standby Power @ 0.5W load vs. AC Line Input Voltage
(Equipment: Yokogawa WT210 power meter – using integration mode)

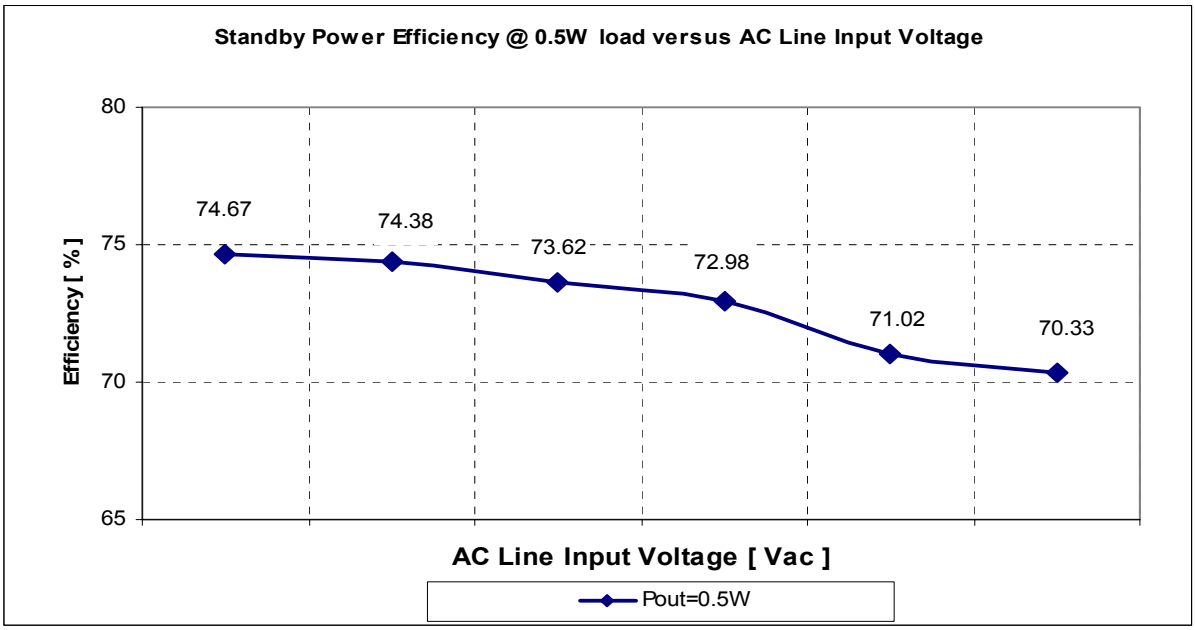

Figure 10 – Standby Power Efficiency @ 0.5W load vs. AC Line Input Voltage

10.3 Line Regulation

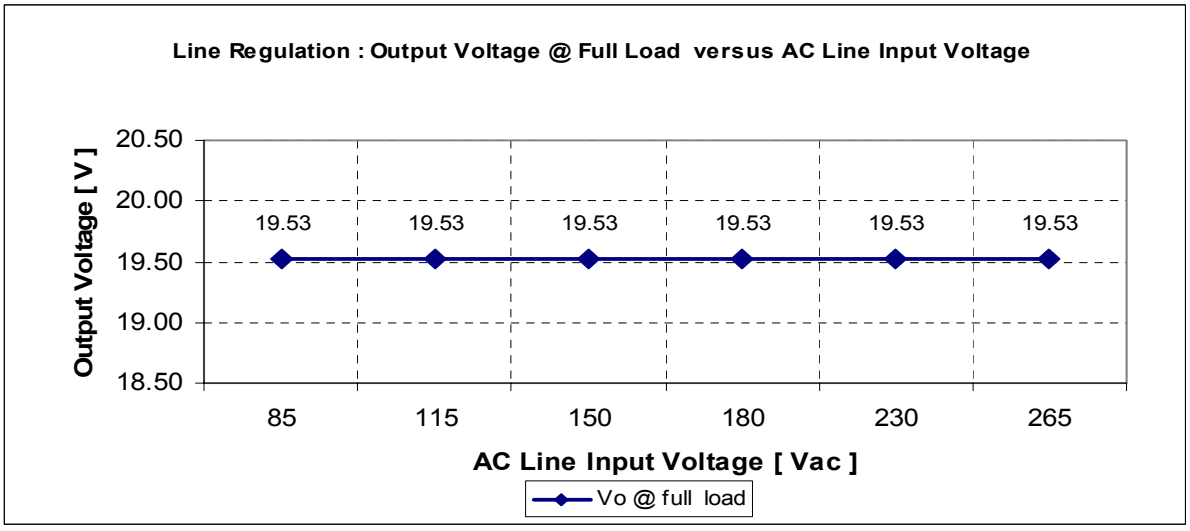

Figure 11 – Line Regulation vs. AC Line Input Voltage

10.4 Load Regulation

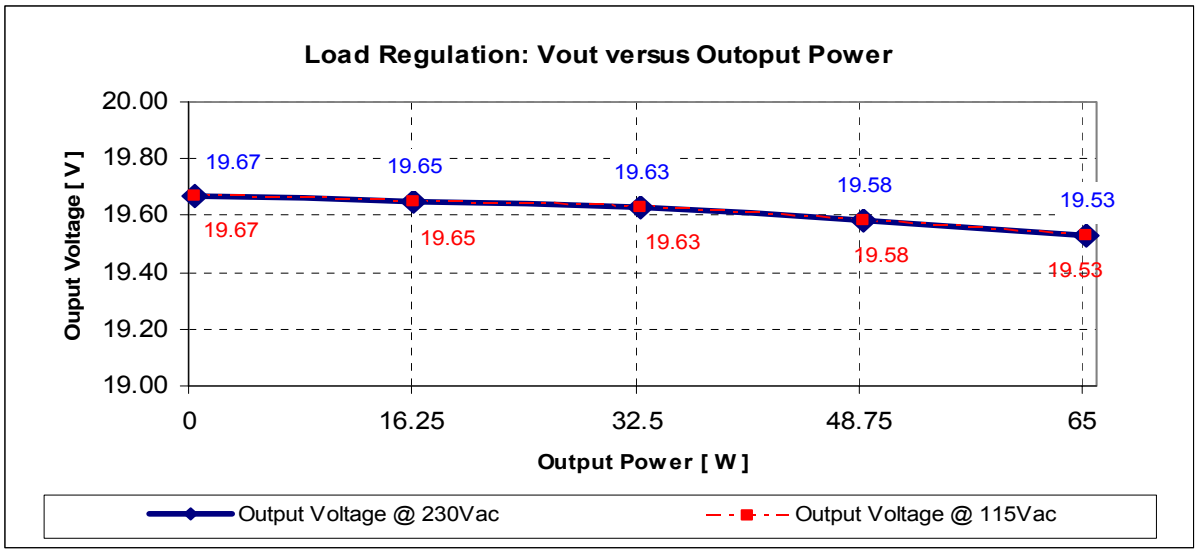

Figure 12 – Load Regulation vs. AC Line Input Voltage

10.5 Max. Overload Output Power

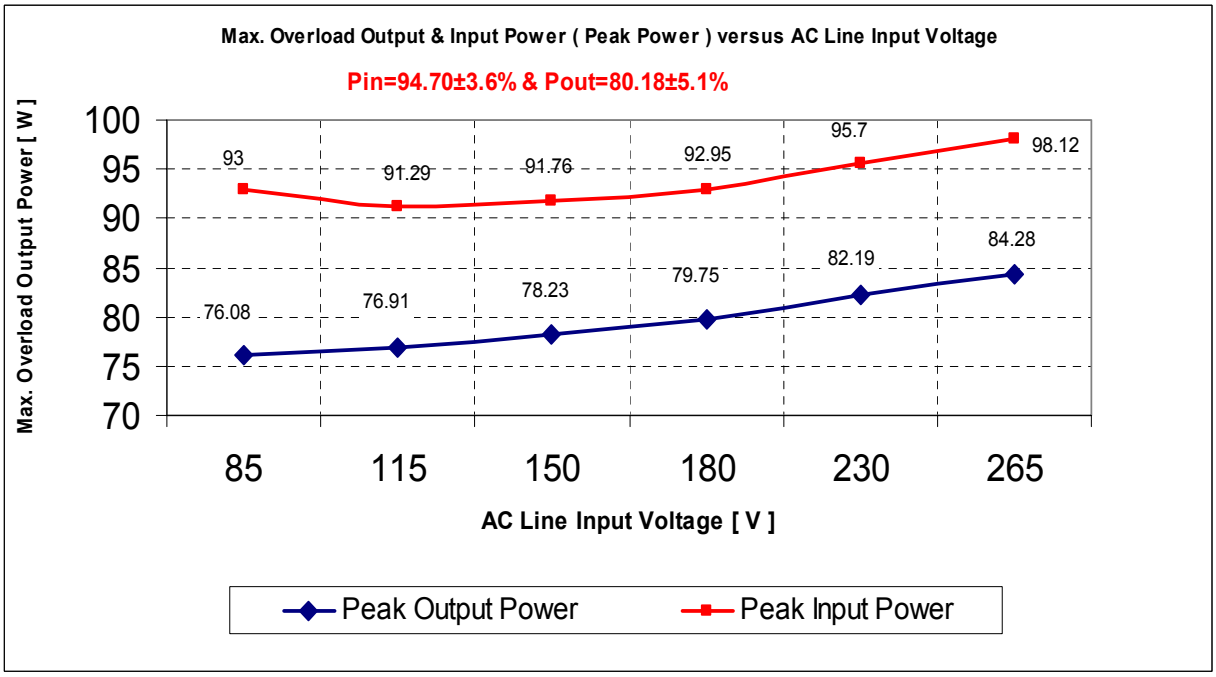

Figure 13 – Overload Output Power (Over Current Shut Off Threshold) vs. AC Line Input Voltage

10.6 ESD

Pass (EN61000-4-2) 20kV for contact discharge.

10.7 Lightning Surge

Pass* (EN61000-4-5) 6kV for line to earth.

*Add SG1 & SG2 (DSP-301N-S008)

10.8 Conducted EMI test

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN55022 class B. The demo board was set up at maximum load with input voltage of 115Vac and 230Vac.

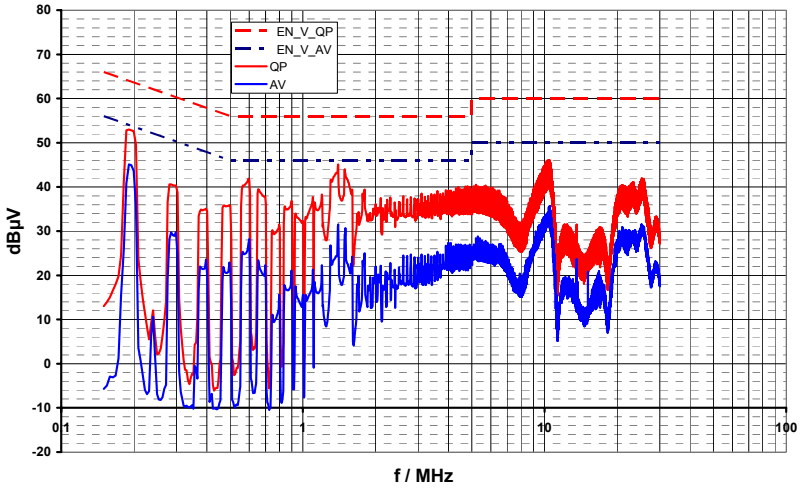

Figure 14 – Max. Load (65W) with 115 Vac (Neutral)

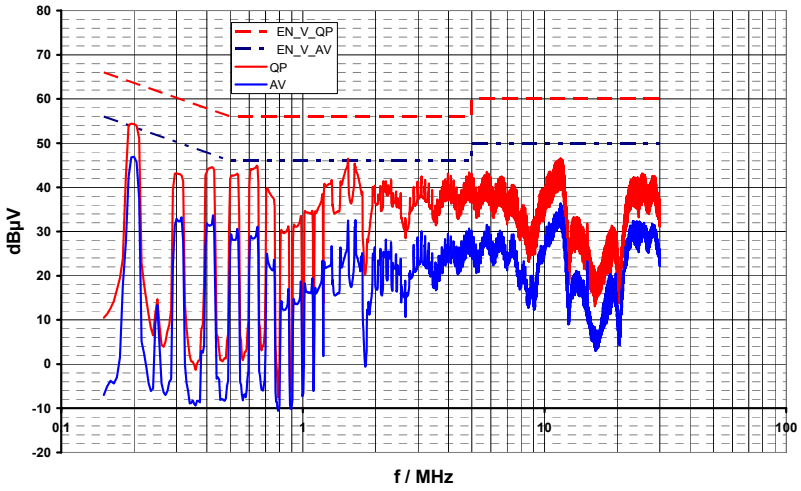

Figure 15 – Max. Load (65W) with 230 Vac (Neutral)

11 Waveforms and Scope Plots

All waveforms and scope plots were recorded with a LeCroy 6050 oscilloscope

11.1 Startup waveforms @ full load

<table>
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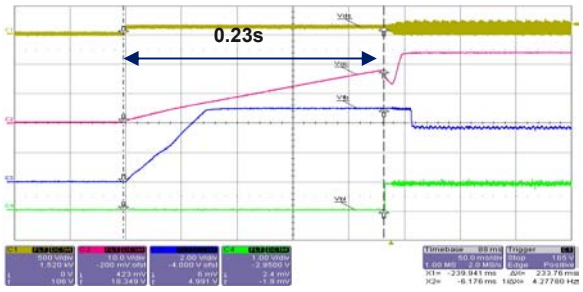
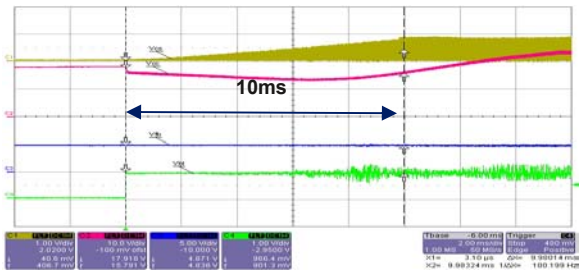
<td> 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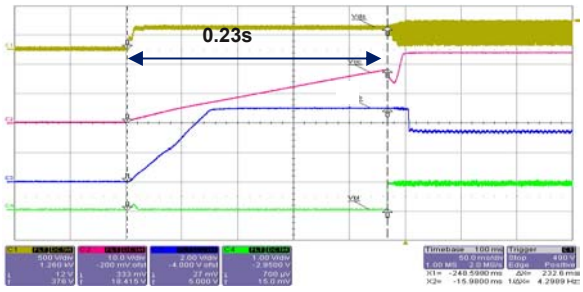
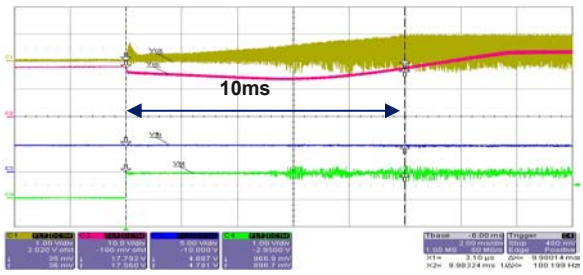
<td> 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<tr>
<td>Channel 1; C1 : Drain Source voltage (V_{DS})
Channel 2; C2 : Supply Voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : BL Voltage (V_{BL})</td>
<td>Channel 1; C1 : Drain Source voltage (V_{DS})
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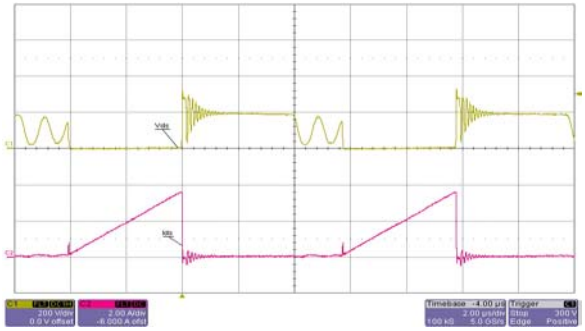
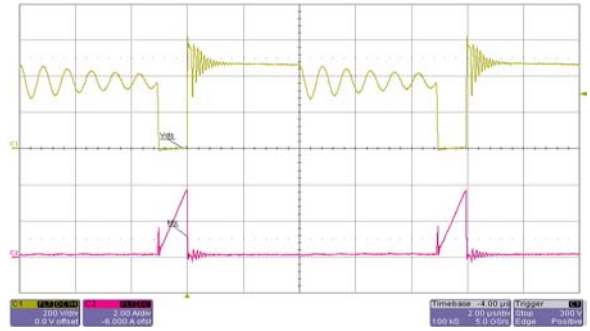
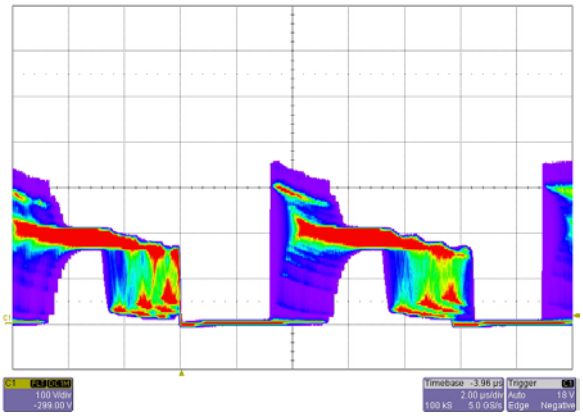
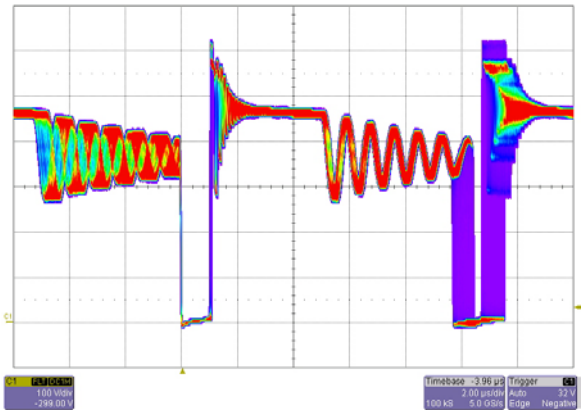
</tr>
<tr>
<td>Startup time = 0.23s, Soft start time = 10ms</td>
<td>Startup time = 0.23s, Soft start time = 10ms</td>
</tr>
<tr>
<td>Figure 16 – Startup @ Vin=85Vac and 65W load</td>
<td>Figure 17 – Startup @ Vin=265Vac and 65W load</td>
</tr>
</table>

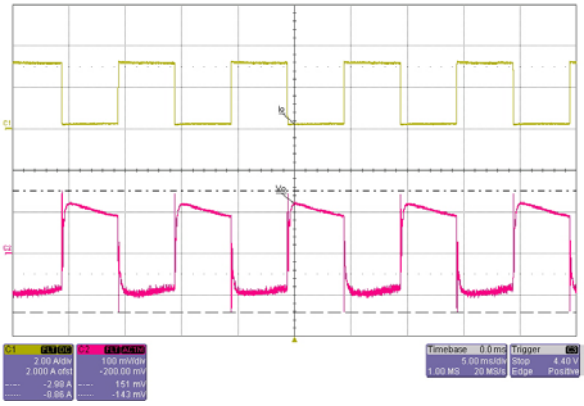
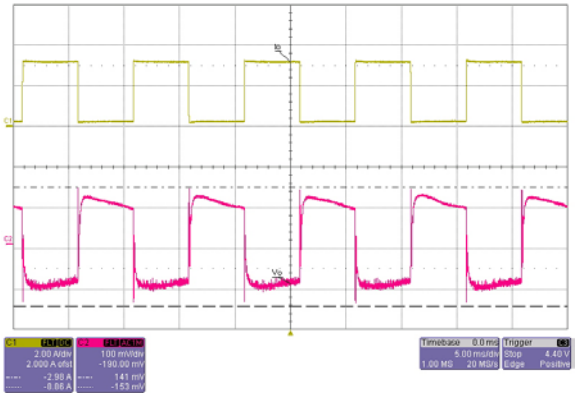
11.2 Drain-Source voltage and current @ full load

<table>
<tr>
<td>  </td>
<td>  </td>
</tr>
<tr>
<td>Channel 1; C1 : Drain Source Voltage (V_{DS})
Channel 2; C2 : Drain Source Current (I_{DS})</td>
<td>Channel 1; C1 : Drain Source Voltage (V_{DS})
Channel 2; C2 : Drain Source Current (I_{DS})</td>
</tr>
<tr>
<td>Duty cycle = 41.6%</td>
<td>Duty cycle = 10.7%</td>
</tr>
<tr>
<td>Figure 18 – Operation @ Vin = 85Vac and 65W load</td>
<td>Figure 19–Operation @ Vin = 265Vac and 65W load</td>
</tr>
</table>

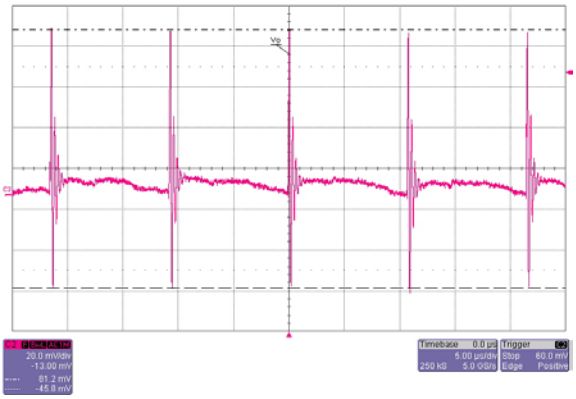
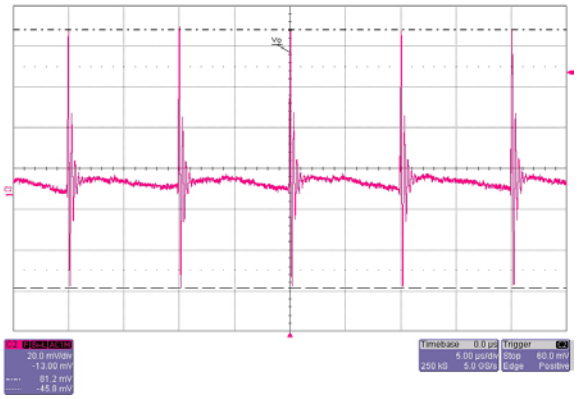
11.3 Frequency jittering

	
Channel 1; C1 : Drain Source voltage (V_{DS})	Channel 1; C1 : Drain Source voltage (V_{DS})
Frequency changing from 95.6kHz ~ 102kHz, Jitter period is set at 4ms internally	Frequency changing from 95.6kHz ~ 102kHz, Jitter period is set at 4ms internally
Figure 20 – Frequency change shown at V_{DS} @ Vin=85Vac and 65W Load	**Figure 21** – Frequency change shown at V_{DS} @ Vin=265Vac and 65W Load

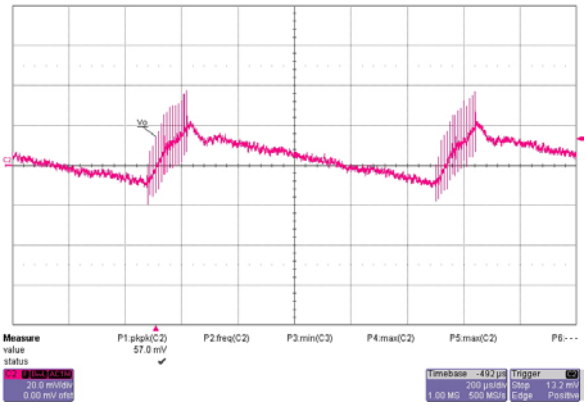
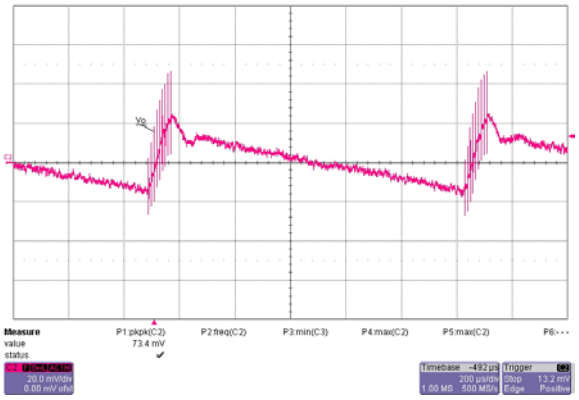
11.4 Load transient response (Load jump from 10% to 100%)

	
Channel 2; C1 : Output Current (I_O) Channel 2; C2 : Output Voltage (V_O)	Channel 2; C1 : Output Current (I_O) Channel 2; C2 : Output Voltage (V_O)
$V_{ripple\_pk\_pk}$= 294mV(Load 10% to 100%,100Hz,0.4A/µS slew rate), No Oscillation	$V_{ripple\_pk\_pk}$= 294mV(Load 10% to 100%,100Hz,0.4A/µS slew rate), No Oscillation
Figure 22– Load jump @ Vin=85Vac from 10% to 100%	**Figure 23** – Load jump @ Vin=265Vac from 6W to 60W load

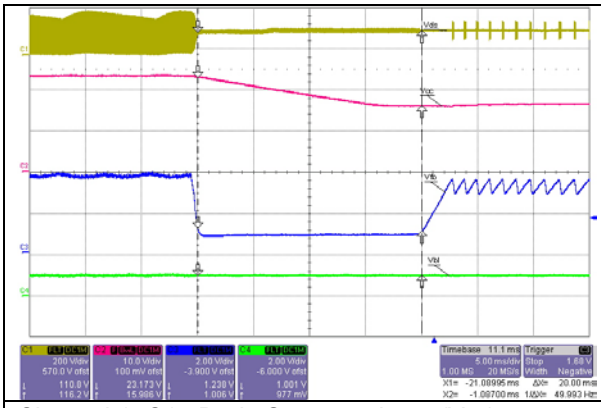
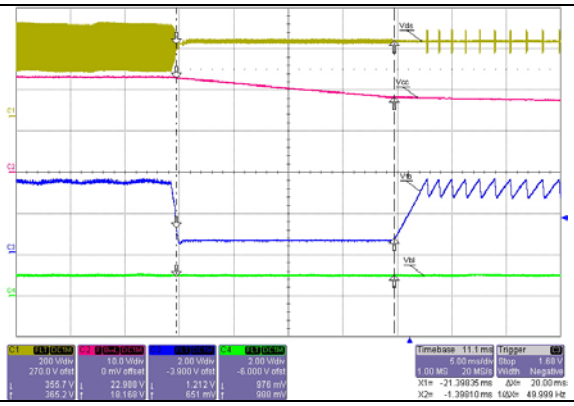
11.5 Output ripple voltage @ Full Load

	
Channel 2; C2 : Output Ripple Voltage (V_O)	Channel 2; C2 : Output Ripple Voltage (V_O)
$V_{ripple\_pk\_pk}$= 127mV (Probe terminal end with decoupling capacitor of 0.1uF(ceramic) + 1uF(Electrolytic),20MHz)	$V_{ripple\_pk\_pk}$= 127mV (Probe terminal end with decoupling capacitor of 0.1uF(ceramic) + 1uF(Electrolytic),20MHz)
Figure 24 – Output voltageripple @ 85Vac and 65W load	**Figure 25** – Output voltageripple @ 265Vac and 65W load

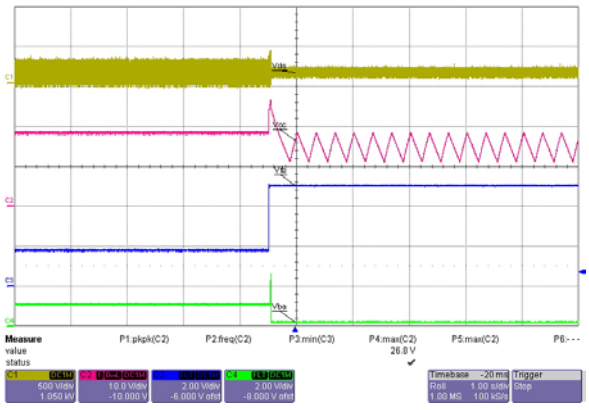
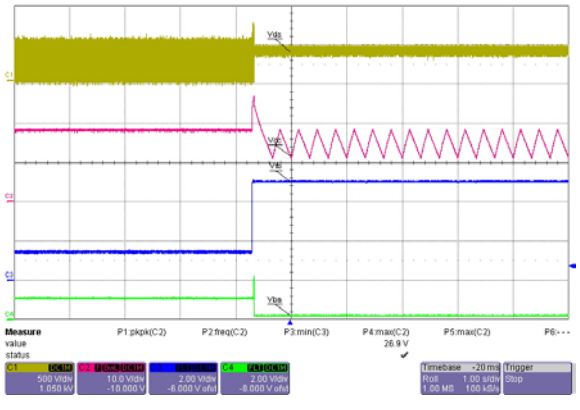
11.6 Output ripple voltage during burst mode @ 1W Load

	
Channel 2; C2 : Output Ripple Voltage (V_O)	Channel 2; C2 : Output Ripple Voltage (V_O)
$V_{ripple\_pk\_pk}$= 57mV (Probe terminal end with decoupling capacitor of 0.1uF(ceramic) + 1uF(Electrolytic),20MHz)	$V_{ripple\_pk\_pk}$= 73.4mV (Probe terminal end with decoupling capacitor of 0.1uF(ceramic) + 1uF(Electrolytic),20MHz)
Figure 26 – Output ripple voltage @ Vin=85Vac and 1W load	**Figure 27** – Output ripple voltage @ Vin=265Vac and 1W load

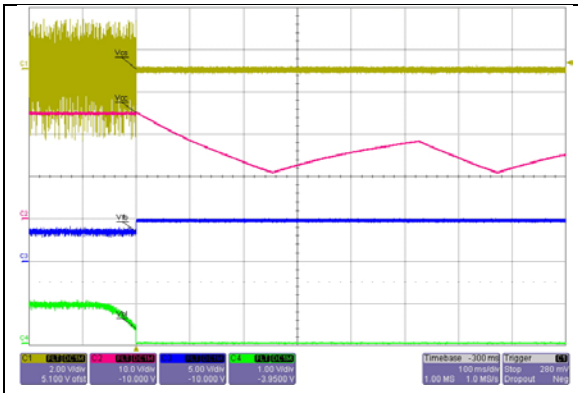
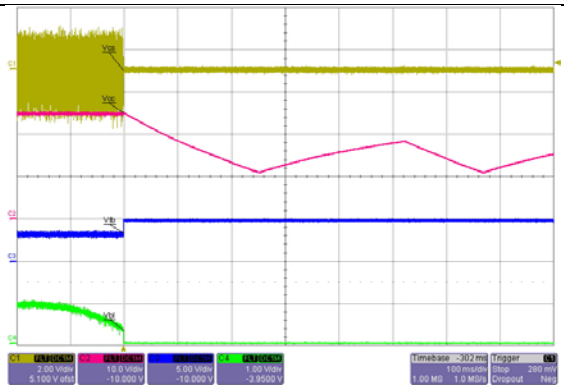
11.7 Active burst mode @ 1W load

	
Channel 1; C1 : Drain Source voltage (V_{DS}) Channel 2; C2 : Supply Voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : BL Voltage (V_{BL})	Channel 1; C1 : Drain Source voltage (V_{DS}) Channel 2; C2 : Supply Voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : BL Voltage (V_{BL})
Load change from 3.34A to 0.5A, blanking time to enter burst mode is 20ms	Load change from 3.34A to 0.5A, blanking time to enter burst mode is 20ms
Figure 28 – Active burst mode @ Vin=85Vac	**Figure 29** – Active burst mode @ Vin=265Vac

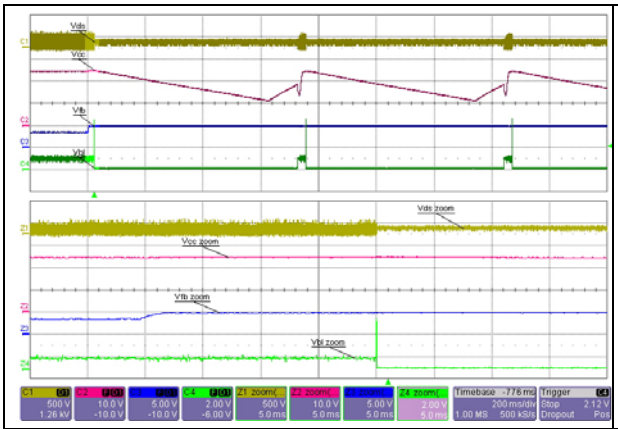
11.8 Vcc overvoltage protection - Latched Off

	
Channel 1; C1 : Drain Source voltage (V_{DS}) Channel 2; C2 : Supply Voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : BL Voltage (V_{BL})	Channel 1; C1 : Drain Source voltage (V_{DS}) Channel 2; C2 : Supply Voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : BL Voltage (V_{BL})
R16 disconnected during system operating at 0.5A load,System enters to latched off mode due to Vcc OVP	R16 disconnected during system operating at 0.5A load,System enters to latched off mode due to Vcc OVP
Figure 30 – Vcc overvoltage protection @ Vin=85Vac	**Figure 31** – Vcc overvoltage protection @ Vin=265Vac

11.9 External protection enable (Mosfet OTP) – Latched Off

	
Channel 1; C1 : Drain Source voltage (V_{DS}) Channel 2; C2 : Supply Voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : BL Voltage (V_{BL})	Channel 1; C1 : Drain Source voltage (V_{DS}) Channel 2; C2 : Supply Voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : BL Voltage (V_{BL})
DUT is operating at full load and ambient is 80°C, system enters latch off mode when V_{BL} <0.33 (measured heatsink temperature is 103°C & mosfet surface temperature is 107°C)	DUT is operating at full load and ambient is 80°C, system enters latch off mode when V_{BL} <0.33 (measured heatsink temperature is 103°C & mosfet surface temperature is 107°C)
Figure 32 – External latch off enable(Mosfet OTP)@ 85Vac	**Figure 33** – External latch off enable(Mosfet OTP) @ 265Vac

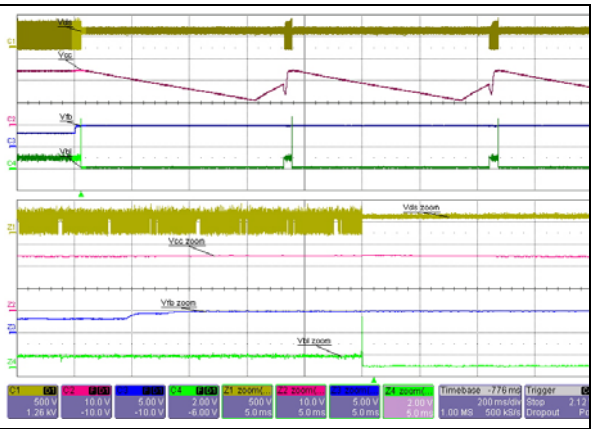
11.10 Over load protection without/with extended blanking time-Auto Restart



Channel 1; C1 : Drain Source voltage (V_{DS})
Channel 2; C2 : Supply Voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : BL Voltage (V_{BL})

Step load from 3.34 to 4.5A, system enters to auto restart mode when V_{FB} > 4.2V and V_{BL} > 4.0V and 20ms blanking time(Cbl=100pF)

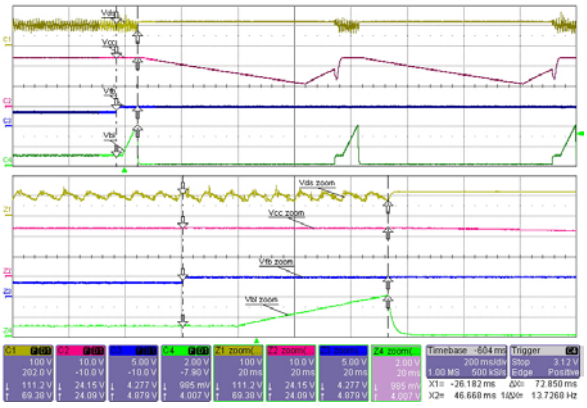
Figure 34 – Overload protection without extended blanking time @ 85Vac



Channel 1; C1 : Drain Source voltage (V_{DS})
Channel 2; C2 : Supply Voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : BL Voltage (V_{BL})

Step load from 3.34 to 4.5A, system enters to auto restart mode when V_{FB} > 4.2V and V_{BL} > 4.0V and 20ms blanking time(Cbl=100pF)

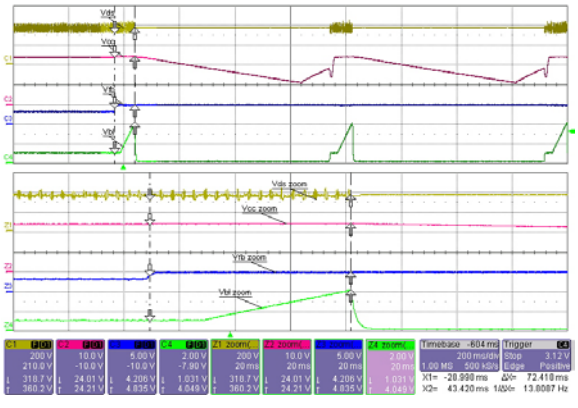
Figure 35– Overload protection without extended blanking time @ 265Vac



Channel 1; C1 : Drain Source voltage (V_{DS})
Channel 2; C2 : Supply Voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : BL Voltage (V_{BL})

Step load from 3.34 to 4.5A, system enters to auto restart mode when V_{FB} > 4.2V and V_{BL} > 4.0V and 72ms blanking time

Figure 36 – Overload protection with extended blanking time @ 85Vac(Cbl=0.22µF)

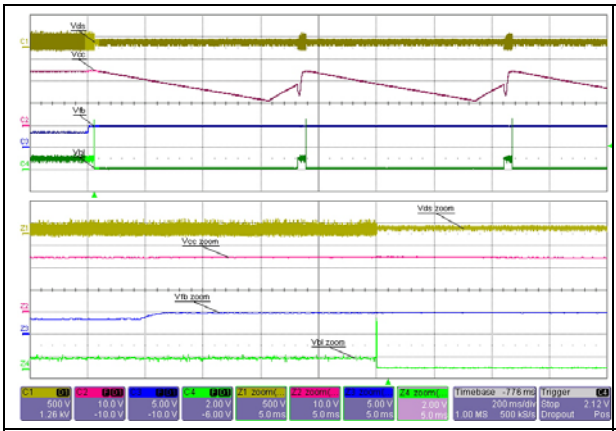
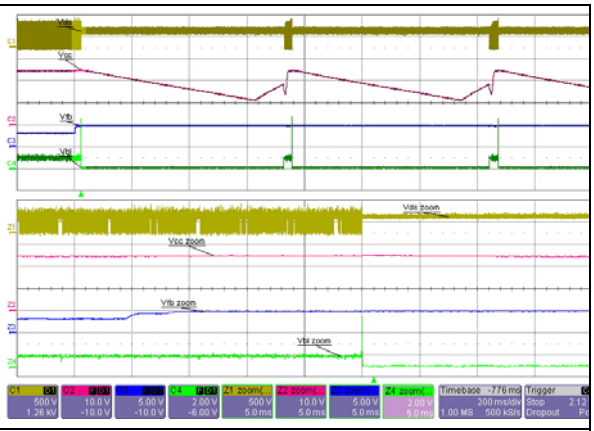


Channel 1; C1 : Drain Source voltage (V_{DS})
Channel 2; C2 : Supply Voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : BL Voltage (V_{BL})

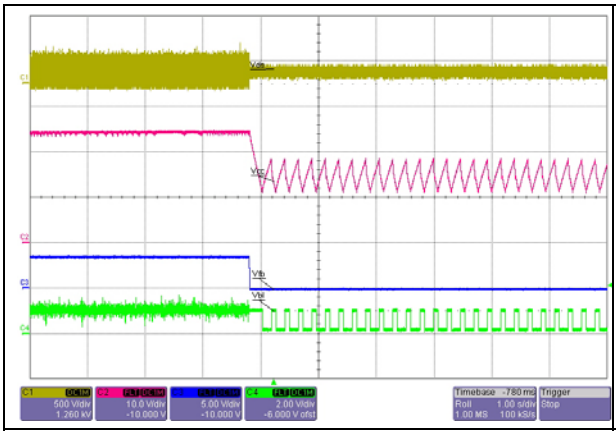
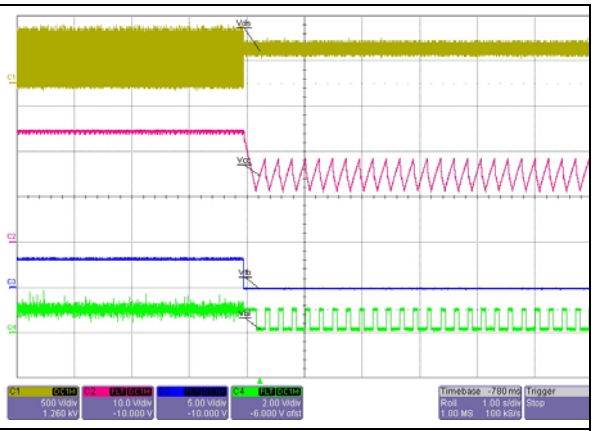
Step load from 3.34 to 4.5A, system enters to auto restart mode when V_{FB} > 4.2V and V_{BL} > 4.0V and 72ms blanking time

Figure 37– Overload protection with extended blanking time @ 265Vac(Cbl=0.22µF)

11.11 Open loop protection – Auto Restart

	
Channel 1; C1 : Drain Source voltage (V_{DS}) Channel 2; C2 : Supply Voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : BL Voltage (V_{BL})	Channel 1; C1 : Drain Source voltage (V_{DS}) Channel 2; C2 : Supply Voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : BL Voltage (V_{BL})
R16 disconnected during system operating at 3.34A load, system enters to auto restart mode when V_{FB} > 4.2V and V_{BL} > 4.0V and 20ms blanking time (Over load protection)	R16 disconnected during system operating at 3.34A load, system enters to auto restart mode when V_{FB} > 4.2V and V_{BL} > 4.0V and 20ms blanking time (Over load protection)
Figure 38 – Open loop protection @ 85Vac	**Figure 39** – Open loop protection @ 265Vac

11.12 Vcc under voltage/Short optocoupler – Auto Restart

	
Channel 1; C1 : Drain Source voltage (V_{DS}) Channel 2; C2 : Supply Voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : BL Voltage (V_{BL})	Channel 1; C1 : Drain Source voltage (V_{DS}) Channel 2; C2 : Supply Voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : BL Voltage (V_{BL})
Shorting the transistor of the opto-coupler(IC2), System enters to Auto Restart mode when V_{cc}<10.5V	Shorting the transistor of the opto-coupler(IC2), System enters to Auto Restart mode when V_{cc}<10.5V
Figure 40 – Vcc under voltage/Short optocoupler protection @ 85Vac	**Figure 41** – Vcc under voltage/Short optocoupler protection @ 265Vac

12 References

[1] Infineon Technologies, Datasheet “F3 PWM controller ICE3AS03LJG Off-Line SMPS Current Mode Controller with Integrated 500V Startup Cell (Latched and Frequency Jitter Mode)”

[2] Infineon Technologies, Application Note “AN-SMPS-ICE2xXXX-1 CoolSET™ ICE2xXXX for OFF-Line Switch Mode Power Supply (SMPS)”

[3] Infineon Technologies, Application Note “ICE3BS03LJG F3 Fixed Frequency PWM Controller (Latch & Jitter version) Design Guide”